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(54) DEVICE AND METHOD FOR MULTIPLEXING SIGNAL

(57) Modulated signals inputted through terminals 11_1-11_n are converted in frequency into signals of mutually different frequency bands by means of frequency converting means 12_1-12_n. The converted signals are supplied to a power combining means (16) respectively through variable attenuators 21_1-21_n, multiplexed and outputted. Part of the multiplexed output is extracted and a level detecting means (23) detects the envelope power level. A control means (24) inputs the level L detected by the detecting means (23). When the level L exceeds the level L_s which is k-times (k is about 4 or 5) higher than the average power of the multiplexed signals, the control means (24) attenuates the average power of the modulated signals by a fctor of k/n during the period of about $1/\Delta F_0$ (sec.) (where ΔF_0 is the bandwidth frequency of the multiplexed signals) by means of the attenuators 21_1-21_n.

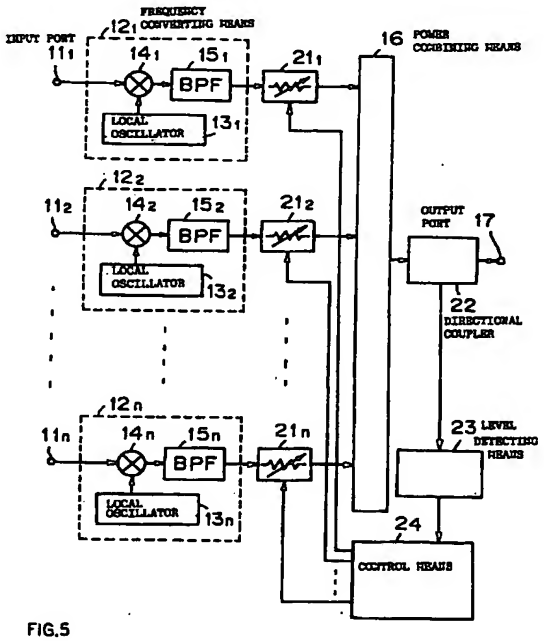

FIG.5

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Description

TECHNICAL FILED

The present invention relates to a signal multiplexer which combines the power of multiple, modulated and different frequency-band signals (hereinafter referred to simply as modulated signals). The signal multiplexer is applied to, for example, a multi-carrier transmission system used in mobile communications, satellite communications or radio paging systems.

BACKGROUND ART

Fig. 1 illustrates a conventional signal multiplexer. Input signals from input port 11_1 to 11_n are converted by frequency converting means 12_1 to 12_n into signals of different frequency bands, respectively. In each frequency converting means 12_i ($i = 1, 2, ..., n$), the frequency of the input signal from the input port 11_i is mixed by a multiplier 14_i with the frequency f_i of a local signal from a local oscillator 13_i and a desired frequency band f_i' is filtered by a band-pass filter 15_i from the mixed output as the output of the frequency converting means 12_i. Here, the input signal from the input port 11_i is, for example, a baseband signal which is BPSK modulated, QPSK modulated, QAM modulated or an intermediate frequency signal which is modulated by a certain type of modulation scheme. The output signals from the frequency converting means 12_1 to 12_n are linearly combined by power combining means 16, which provides the combined output to an output port 17. The power combining means 16 linearly combines multiple, modulated and different frequency-band signals that are provided from n input channels and is constructed by a transformer circuit or hybrid circuit. In this way, the n-channel input signals are multiplexed in the frequency space. The multiplexed signal is output from output port 17 as a multi-carrier signal, which is composed of different frequency-band signals and has equally spaced carrier components. In some cases, the band-pass filters 15_1 to 15_n are omitted and instead a band-pass filter is provided at the output side of the power combining means 16.

Fig. 2 shows the basic principle of a conventional m-ary FSK signal multiplexer for $m = 2$. For $m > 2$, the configuration of the multiplexer is the same as in the case where $m = 2$, except that m local oscillators are used. This conventional multiplexer comprises n ($n \geq 2$) m-ary FSK modulators 5_i ($i = 1, 2, ..., n$) corresponding to n channels and a power combining means 6. Each m-ary FSK modulator 5_i is composed of input ports 1_i, m ($m = 2$ in this example) local oscillators 2_i and 3_i which oscillate at different frequencies, and signal switching means 4_i which selects and outputs either one of the outputs from the oscillators 2_i and 3_i in accordance with the code of the input signal to the input port 1_i. The output signals from the m-ary FSK modulators 5_i are different in frequency band and are linearly combined by the power combining means 6 constructed by a transformer circuit or hybrid circuit, and an FSK signal multiplexed in the frequency space is provided at an output port 7.

The local oscillators 2_i and 3_i are all shown to operate independently of each other. However, in some cases, reference frequency oscillating means is provided and its output is split into all the oscillators 2_i and 3_i in order to improve the frequency accuracy of all the local oscillators 2_i and 3_i.

As shown in Fig. 3, the m-ary FSK modulator 5_i may sometimes be constructed by one oscillating means (usually a PLL synthesizer) which is able to change the frequency of the output signal in accordance with the signal at the input port 1_i. The circuit configuration in Fig. 3 is identical with that in Fig. 2 except the provision of reference frequency oscillating means 8 and the configuration of the m-ary FSK modulator 5_i. The m-ary FSK modulator (PLL frequency synthesizer) 5_i in Fig. 3 is made up of low-pass filter means 9_i, amplifying means 10_i, a voltage-controlled oscillator (VCO) 41_i, a variable frequency divider 42_i and a phase comparator 43_i. The phase comparator 43_i compares the phases of both signals fed thereto from the reference frequency oscillating means 8 and the variable frequency divider 42_i. Then, the phase comparator 43_i outputs a voltage corresponding to the phase difference between the both signals. The voltage corresponding to the phase difference is applied to a control port of the VCO 41_i via the low-pass filter means 9_i and the amplifying means 10_i. The frequency dividing ratio ($1/N_i$) of the variable frequency divider 42_i is set in accordance with the input signal S_i; the VCO 41_i outputs a signal of an oscillating frequency $N_i f_i = N_i f_r$ corresponding to the input signal S_i.

It is presupposed hitherto that the above n m-ary FSK modulators 5_i are operated at different center frequencies (carrier frequencies). However, in some instances, it may employ a construction wherein the n m-ary FSK modulators 5_i are operated at the same center frequency (carrier frequency) and frequency converting means is interposed between the outputs of the m-ary FSK modulators 5_i and the power combining means 6 in order to convert the frequency of the output signal from each m-ary FSK modulator 5_i to a desired frequency band. The frequency converting means is composed of a frequency synthesizer (or local oscillator), a mixer and band-pass filter means.

Note the envelope power of the multiplexed modulated signal that is obtained at the output port 17 in Fig. 1 in the application of the conventional signal multiplexer to actual communication; since the phases of individual modulated signals are variously distributed in specific ranges, instantaneous phases of the modulated signals readily coincide and the voltages of the instantaneous modulated signals are combined in-phase. As a result, the envelope power sharply increases and a peak envelope power (PEP), which is significantly higher than the average power level of the envelope power, is often generated.

Also in case of the signal obtained by multiplexing individual m-ary FSK modulated signals, instantaneous phases of the modulated waves generated by the m-ary FSK modulators readily coincide according to the frequencies of the modulated waves and their phases at the time of frequency switching, and at that instant, their voltages are combined in-phase. In consequence, a peak envelope power (PEP) which is drastically higher than the average power P_a of the envelope power occurs as shown in Fig. 4. The peak envelope power PEP can increase up to n times (where n is the number of multiplexing) the average power P_a.

In either case, if an amplifier is provided at the output port of the conventional signal multiplexer to amplify the multiplexed signal with a low level of distortion, although the peak envelope power PEP is substantially higher than the average power level of the envelope power, the required saturation power of the amplifier needs to be set larger than the average power level of the envelope power at least by a multiple of the number of multiplexing -- this poses the problem of hindering miniaturization and power saving of the amplifier.

As a solution to this problem, there is disclosed in Japanese Pat. Laid-Open Gazette No. 30537/92 a construction in which a phase shifter is provided for each channel and its phase shift amount is suitably set to decrease the peak envelope power. This method makes it possible to prevent a large peak from appearing in the envelope power when each channel is not modulated, and the method is effective for a modulation scheme that holds the initial phase of the carrier as in the case of double-sideband amplitude modulation. However, since a signal modulated by a modulation scheme such as phase or frequency modulation undergoes a change in the carrier phase by the modulated input, a large peak can occur in the peak envelope power of the multi-carrier signal. Further, it is disclosed in Fig. 7 of the above-mentioned gazette to detect the power of a specific frequency of the multi-carrier signal and control the phase shifter of each channel. However, the gazette does not concretely state how each phase shifter is controlled in accordance with the detected power; hence, the invention of the gazette cannot be compared with the present invention in this respect.

In Japanese Pat. Laid-Open Gazette No. 204773/94 (U.S. Patent Application No. 963784 filed October 20, 1992) there is disclosed a method that monitors the peak envelope power (PEP) of the multi-carrier signal and, when the PEP exceeds a predetermined value, adjusts the shift amount of the phase shifter in each channel to reduce the peak envelope power PEP of the multi-carrier signal. With this method, since it is not clear how the phase shift amount in each channel is controlled as in the case with the first-mentioned Japanese Laid-Open Gazette, the shift amount of the phase shifter is slightly increased or decreased for each channel, then a check is made to see if the peak envelope power PEP of the multi-carrier signal at that time increases or decreases and the shift amount is controlled to decrease the peak envelope power. Thus, in a very short period of time during which a peak appears in the peak envelope power, the above-mentioned control needs to be effected for each phase shifter; namely, this method requires many high-speed processes and hence is not practical.

In Japanese Pat. Laid-Open Gazette No. 204959/94 (U.S. Patent Application No. 964596 filed October 20, 1992), there is disclosed a method that detects the ratio of the peak envelope power PEP to the average power of the multi-carrier signal (PEP/average power) and, when this ratio exceeds a predetermined value, controls the phase shifter of each channel to reduce the peak envelope power PEP. This method also involves many high-speed processes and hence is not practical.

Moreover, in Seymour SHLIEN, "Miniaturization of the Peak Amplitude of a Waveform," Signal Processing 14 (1988), pp. 91-93, there is made a proposal that uses a steepest descent method to search an initial phase condition that reduces the peak envelope power for a binary FSK multi-carrier signal of 12 carriers of the same amplitude. No concrete circuit configuration is shown; hence, it is not clear how the proposal is implemented.

It is an object of the present invention to provide a signal multiplexer which prevents a sharp increase in the peak envelope power (PEP) of the multiplexed signal (a multi-carrier signal).

Another object of the prevent invention is to provide a signal multiplexer which prevents a sharp increase in the peak envelope power of the multiplexed signal and produces the signal with a relatively low level of distortion.

Another object of the present invention is to provide a signal multiplexer which multiplexes an m-ary FSK signal and prevents a sharp increase in the peak envelope power of the multiplexed FSK signal.

Still another object of the present invention is to provide a signal multiplexer which multiplexes a plurality of modulated signals and, when the number of signals to be multiplexed increases, prevents a sharp increase in the peak envelope power of the multiplexed signal.

DISCLOSURE OF THE INVENTION

According to a first aspect of the present invention, in a device which multiplexes modulated signals from n input systems by power combining means, variable attenuator means are respectively connected in series with m' of n input ports of the power combining means for the n (where $m' \leq n$) input systems, the envelope power level of the signal combined by the power combining means or the multiplexed signal is detected by envelope power level detecting means, and when the detected envelope power level exceeds a predetermined value, a predetermined amount of attenuation is set by control means in m (where $m \leq m'$) of the m' var-

iable attenuator means for a predetermined period of time.

According to a second aspect of the present invention, the device is identical in construction with the device according to the first aspect except providing variable attenuator means between the power combining means and the output port instead of providing the variable attenuator means for each input systems in the first aspect.

The control means sets a predetermined amount of attenuation for a predetermined period of time when the envelope power level exceeds the predetermined value in succession a predetermined number of times. Alternatively, the control means sets a predetermined amount of attenuation for a predetermined period of time when the envelope power level exceeds a predetermined value for more than a predetermined period of time.

According to a third aspect of the present invention, in a method which linearly combines n modulated signals into a multiplexed signal, the envelope power level L of the multiplexed signal is detected, then the detected level L is compared with a predetermined level L_s, and if $L > L_s$, m of the n (where $m \leq n$) modulated signals are attenuated as predetermined for a predetermined period of time.

According to a fourth aspect of the present invention, in a method which linearly combines n modulated signals into a multiplexed signal, the envelope power level L of the multiplexed signal is detected, then the detected level L is compared with a predetermined level L_s, and if $L > L_s$, the multiplexed signal is attenuated as predetermined for a predetermined period of time.

In the third and fourth aspects of the invention, when $L > L_s$, the count value is incremented by one, and when the count value M reaches a predetermined value M_0, the predetermined amount of attenuation is provided; if $M < M_0$, then the process goes back to the level detection step, and if $L < L_s$, then the count value M is made zero and the process returns to the level detection step.

In the third and fourth aspects of the invention, if $L > L_s$, then the counting of time T begins and when the time T reaches a predetermined value T_0, the predetermined amount of attenuation is provided; if $T < T_0$, then the process immediately returns to the level detection step, and if $L < L_s$, the process goes back to the level detection step after resetting the count value T to zero.

In the first and second aspects of the invention the attenuator means is controlled when the envelope power level of the multiplexed signal exceeds a predetermined value, but according to fifth and sixth aspects of the present invention, the average power of the multiplexed signal is detected by average power detecting means, and when the ratio of the detected envelope power level to the detected average power exceeds a predetermined value, the attenuator means is controlled.

According to a seventh aspect of the present invention, in an FSK signal multiplexer which combines the output signals from n (n-channel) m-ary FSK modulating means (where n and m are both integers equal to or greater than 2) by power combining means; the n m-ary FSK modulating means shift their output frequencies in accordance with the sign of the input signals thereto based upon a common reference frequency signal from reference frequency oscillating means, there are provided variable phase shifter means for shifting the phase of the modulated signal from each m-ary FSK modulated means and control means for setting the phase shift amount of the variable phase shifter means so that the peak envelope power of the output from the power combining means becomes small in accordance with the combination of symbols of the n input signals in synchronization with the timing at which the m-ary FSK modulating means switch their output frequencies in accordance with the input signals thereto.

The m-ary FSK modulating means each comprise m oscillators of different oscillation frequencies and signal switching means which selects one of the m oscillators in accordance with the sign of the input signal thereto and outputs the oscillation signal from the selected oscillator. Alternatively, each m-ary FSK modulation means is constructed by a PLL frequency synthesizer, or the m-ary FSK modulating means and the variable phase shifter means in each channel are constructed by a direct digital frequency synthesizer (DDS).

The input signal in each channel is branched by branching means to both one (common) control means and the corresponding m-ary FSK modulating means, and delay means is inserted in the signal path between the branching means and the m-ary FSK modulating means.

In the cases where each m-ary FSK modulation means is constructed by m oscillators or by a PLL frequency synthesizer, the variable phase shifter means is disposed at the output side of each m-ary FSK modulating means or is connected in series with the reference frequency signal input port of each m-ary FSK modulating means. The control signal for the variable phase shifter means is processed so that the phase of the modulated signal remains continuous before and after its frequency change caused by a change in the sign of the input signal.

The seventh aspect of the invention is combined with the first or second aspect.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a conventional signal multiplexer.

Fig. 2 is a block diagram showing the principles of a conventional FSK signal multiplexer.

Fig. 3 is a block diagram illustrating a concrete example of the conventional FSK signal multiplexer.

Fig. 4 is a diagram showing examples of envelope power waveforms of FSK multiplexed signals.

Fig. 5 is a block diagram illustrating an embodiment according to a first aspect of the present invention.

Fig. 6A is a flowchart showing an example of the control operation of control means 24 in Fig. 5 and the procedure of an embodiment according to a third aspect of the invention, and Fig. 6B is a timing chart showing examples of attenuating operations of variable attenuators 21_1 to 21_n in the control operation of the control means and the procedure of the embodiment according to the third aspect of the invention.

Fig. 7 is a flowchart showing an example of the control operation of the control means 24 in the first and second aspect of the present invention and procedures of embodiments according to the third and fourth aspects of the invention.

Fig. 8 is a flowchart showing an example of the control operation of the control means 24 in the first and second aspects of the present invention and procedures of other embodiments according to the third and fourth aspects of the invention.

Fig. 9 is a block diagram illustrating an embodiment according to the second aspect of the present invention.

Fig. 10 is a block diagram illustrating another embodiment according to the second aspect of the present invention.

Fig. 11 is a block diagram illustrating another embodiment according to the first aspect of the present invention.

Fig. 12 is a block diagram another embodiment according to the second aspect of the present invention.

Fig. 13 is a block diagram illustrating another embodiment according to the first aspect of the present invention.

Fig. 14 is a block diagram illustrating an embodiment according to a fifth (sixth) aspect of the present invention.

Fig. 15 is a block diagram illustrating an embodiment according to a seventh aspect of the present invention.

Fig. 16 is a timing chart showing operations of principal parts of the Fig. 15 embodiment.

Fig. 17 is a block diagram illustrating an embodiment according to the seventh aspect of the invention which employs a PLL frequency synthesizer as an m-ary FSK modulator.

Fig. 18 is a block diagram illustrating another embodiment according to the seventh aspect of the invention which employs a direct digital frequency synthesizer DDS as the m-ary FSK modulator.

Fig. 19 is a block diagram illustrating an example of the basic configuration of the direct digital frequency synthesizer DDS.

Fig. 20 is a block diagram illustrating another embodiment according to the seventh aspect of the invention.

Fig. 21 is a block diagram illustrating another embodiment according to the seventh aspect of the invention.

Fig. 22 is a block diagram illustrating another embodiment according to the seventh aspect of the invention.

Fig. 23 is a block diagram illustrating another embodiment according to the seventh aspect of the invention.

Fig. 24 is a block diagram illustrating another embodiment according to the seventh aspect of the invention.

Fig. 25 is a block diagram illustration another embodiment according to the seventh aspect of the invention.

Fig. 26 is a block diagram illustrating another embodiment according to the seventh aspect of the invention.

Fig. 27 is a block diagram illustrating another embodiment according to the seventh aspect which is combined with the first aspect of the invention.

Fig. 28 is a block diagram illustrating still another embodiment according to the seventh aspect which is combined with the second aspect of the invention.

Fig. 29 is a flowchart showing the procedure in an embodiment according to the third aspect of the invention.

Fig. 30 is a flowchart showing an example of the procedure for computation of the phase shift amount to be set in variable phase shifter means 47_i in the seventh aspect of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

In Fig. 5 there is illustrated an embodiment in accordance with the first aspect of the present invention, in which the parts corresponding to those in Fig. 1 are identified by the same reference numerals. In the present invention: variable attenuators 21_1 to 21_n are provided in output paths of the frequency converting means 12_1 to 12_n, respectively; a directional coupler 22 is disposed at the output side of the power combining means 16; level detecting means 23 is provided to detect the envelope power level of the combined output signal or modulated multiplex signal branched by the directional coupler 22; the detected output from the level detecting means 23 is input into control means 24; and the variable attenuators 21_1 to 21_n are controlled by the control means 24. The variable attenuators 21_1 to 21_n can be easily constructed by PIN diodes and varactor diodes; commercially available products can be also used. The level detecting means 23 can be constructed using a diode and a capacitor and detects the level of the envelope power of the combined output signal from the power combining means 16. The control means 24 comprises, as its basic circuit components, an A/D converter, a microprocessor, a ROM, a RAM and a D/A converter and possesses a function of adjusting the setting points of the variable attenuators 21_1 to 21_n while at the same time monitoring the input signal from the level detector 23. In Fig. 6A there is shown a flowchart for

explaining the control operation of the control means 24.

To begin with, the envelope power level L of the multiplexed signal is detected by the level detecting means 23 (S_1), and it is decided whether the level L exceeds a threshold value L_s (S_2). When the level L is in excess of the threshold values L_s, the amounts of attenuation of the variable attenuators 21_1 to 21_n are set to d [dB] from 0 [dB] (S_3). The operation of the variable attenuators 21_1 to 21_n is limited only to a certain time ΔT as depicted in the timing chart of Fig. 6B; the counting of time (S_4) and the check to see if the time ΔT has elapsed (S_5) are carried out, and after the elapsed time ΔT, the amounts of attenuation of the variable attenuators 21_1 to 21_n are set again to 0 [dB] (S_6), after which control returns to the step of detecting the envelope power level L (S_1). When it is found that the level L does not exceed the threshold value L_s at the step S_2, control only returns to the step S_1 of detecting the envelope power level L and the variable attenuators 21_1 to 21_n are not adjusted.

Letting ΔT_0 (Hz) represent the frequency spacing between adjacent carriers in a multi-carrier signal produced by n multiplexing of modulated signals, the time during which a peak appears in the envelope power of the multi-carrier signal can be estimated by $T_p = 1/((n - 1)\Delta T_0)$ (sec). This is equal to the reciprocal of the bandwidth of the multi-carrier signal. Hence the time ΔT for attenuation in steps S_4 and S_5 may preferably be set to T_p.

In case of setting the threshold value L_s in step S_2 to k (in the range of 1 to 10) times the average power P_a of the multi-carrier signal, the power for each carrier is adjusted by each variable attenuator 21_i to k/n-fold or below. In other words, 10 log (k/n) dB attenuation is provided to the variable attenuator 21_i. From the viewpoint of miniaturization of the amplifier for amplifying the multiplexed signal from the output port 17, it is preferable that k be small, but when k is small, frequent control of the amount of attenuation of the variable attenuator 21_i suppresses the amplitude of each modulated signal, resulting in the signal being distorted accordingly. Thus it is not preferable to set k too small; it is practical that k is in the range of 4 to 5.

With constant or intermittent execution of the sequence of control shown in Fig. 6A, when the envelope power level L of the multiplexed signal exceeds the threshold values Ls, the output level of the multiplexed signal is attenuated by the variable attenuators 21_1 to 21_n for the predetermined time (ΔT), by which it is possible to prevent a sharp increase in the peak envelope power PEP of the multiplexed signal.

The threshold value L_s is set to a value, for example, about four to five times larger than average operation power of a power amplifier which is connected to the output port 17, though not shown, and it is at most 0.1 μs that the envelope power level of the multiplexed signal having a frequency bandwidth of approximately 10 MHz exceeds a value four to five times larger than the above-mentioned average operating power; that part of the envelope corresponding to the period of the envelope power level higher than the threshold value L_s gradually rises just like an elliptic arc. In case of the above-mentioned multiplexed signal, signal distortion poses a problem when the part of the envelope corresponding to the power level higher than the threshold value L_s continues 10 ns or longer. Hence in this example, the envelope power level L is detected very several nanoseconds, and when the envelope power level L exceeds the threshold value L_s, an attenuation of d = 10 dB is set in each of the variable attenuators 21_1 to 21_n for $\Delta T = 0.1$ μs. By effecting the detection control in several nanoseconds or less, low-distortion amplification is made possible even if a small amplifier is used.

With the control scheme shown in Fig. 6A, the variable attenuators 21_1 to 21_n are immediately adjusted when the envelope power level L exceeds the threshold value L_s; however, it is also possible to prevent the variable attenuators 21_1 to 21_n from being automatically controlled in response to an instantaneous increase in the envelope power level L not so much higher than the threshold value L_s, by making provision for adjusting the variable attenuators 21_i when the number of times the envelope power level continuously exceeds the threshold value reaches a predetermined value M_0. In Fig. 7 there is shown, as a flowchart, the control operation of the control means 24 in this instance.

In the first place, a variable M representing the number of times the envelope power level L exceeds the threshold value L_s is initialized (M = 0)(S_{11}). Next, the envelope power level L of the multiplexed signal is detected by the level detecting means 23 (S_1) and a check is made to determine if the level L is higher than the threshold value L_s (S_2). When the level L is higher than the threshold value L_s, the variable M is incremented by one (S_{12}). When the level L is not higher than the threshold value L_s, control only returns to step S_{11} wherein M = 0 and no adjustment is made to the variable attenuators 21_1 to 21_n

When incremented by one, the variable M is compared with a preset value M_0 (S_{13}). If the variable M is equal to the preset value M_0, then the attenuation amount of the variable attenuators 21_1 to 21_n is changed from 0 [dB] to d [dB] (S_3). The variable attenuators 21_1 to 21_n perform the same operations as those described above in respect of Fig. 6A, and after setting the attenuation amount of d for the prescribed time ΔT, control returns to step S_{11}.

When the variable M is not equal to the preset value M_0, control merely returns to step S_1 for the detection of the envelope power level L and no adjustment is made to the variable attenuators 21_1 to 21_n.

With constant or intermittent execution of the above-described sequence of control, the output level of the multiplexed signal is attenuated by the variable attenuators 21_1 to 21_n for the predetermined time ΔT when the envelope power level L of the multiplexed signal continuously exceeds the threshold value L_s M_0

times; so that it is possible to prevent a substantial increase in the peak envelope power of the multiplexed signal. In the multi-carrier signal, since individual carrier signals are modulated independently of the others, the frequency of occurrence of the peak envelope power PEP variously changes in accordance with the modulated carrier signals; it is extremely difficult to estimate how many times the peak envelope power PEP will exceed a predetermined level per unit time. That is to say, the peak envelope power PEP might exceed the predetermined level many times in succession or once at a time. Hence, the number of times M_0 in the above example is twice or more but several times at most.

While the control schemes shown in Figs. 6A and 7 employ, as a decision criterion for adjusting of the variable 21_1 to 21_n, the number of times the envelope power level exceeds the threshold level L_s, the invention of claim 6 uses, as another criterion, the time during which the envelope power level exceeds the threshold level L_s continuously, in which case, if such a duration is equal to or longer than a predetermined time T_0, adjustment is made to the variable attenuators 21_1 to 21_n. In Fig. 8 there is shown as a flowchart for the control operation of the control means 24 in this instance.

The envelope power level L of the multiplexed signal is detected by the level detecting means 23 (S_1) and a check is made to determine if the level is higher than the threshold level L_s (S_2). When the level L is higher than the threshold level L_s, the time T during which L exceeds L_s (S_{21}) is measured and compared with the preset value T_0 (S_{22}). If the level L dose not exceed the threshold value L_s, control simply returns to the step S_1 for the detection of the envelope power level L and no adjustment is made to the variable attenuators 21_1 to 21_n.

When the time T is equal to or longer than the preset value T_0, an attenuation amount of d is set in the variable attenuators 21_1 to 21_n for only the time ΔT, after which control returns to step S_1 for the detection of the envelope power level L. That is, the processing subsequent to step S_3 shown in Fig. 6A is carried out. When it is found in step S_{22} that the T is shorter than the preset value T_0, control simply returns to step S_1 for the detection of the envelope power level L and no adjustment is made to the variable attenuators 21_1 to 21_n.

With constant or intermittent execution of the above-described sequence of control, the output level of the multiplexed signal is attenuated by the variable attenuators 21_1 to 21_n for only the predetermined time ΔT when the time during which the envelope power level L continuously exceeds the threshold value L_s is equal to or longer than the preset value T_0; so that it is possible to prevent a substantial increase in the peak envelope power PEP of the multiplexed signal. In the above case, the value T_o is set to tens of nanoseconds or so. In the embodiment of Fig. 8, since the envelope power level that exceeds the threshold value L_s for an extremely short time does not seriously affect signal distortion, and hence is ignored with a view to reducing the number of times the variable attenuators 21_1 to 21_n are controlled.

Fig. 9 illustrates an embodiment according to the second aspect of the present invention. This embodiment differs from the Fig. 5 embodiment in the provision of only one variable attenuator 21 at a stage posterior to the directional coupler 22 instead of providing the variable attenuators 21_1 to 21_n in the output paths of the frequency converting means 12_1 to 12_n. This embodiment also permits prevention of a substantial increase in the peak envelope power PEP of the multiplexed signal by controlling the variable attenuator 21 alone with a scheme similar to that for controlling the variable attenuators 21_1 to 21_n as described above with reference to Fig. 6A, 7 or 8.

It is also possible to connect only one variable attenuator 21 between the power combining means 16 and the directional coupler 22 as shown in Fig. 10. Alternatively, the variable attenuator 21 may be provided between the power combining means 16 and the output port 17. Further, this embodiment differs from the Fig. 5 embodiment in substituting synthesizers 25_1 to 25_n for the local oscillators 13_1 to 13_n of the frequency converting means 12_1 to 12_n and in driving the synthesizers 25_1 to 25_n by one reference frequency oscillation means 26. With such an arrangement, it is possible to improve the accuracy of the carrier frequency in each of the frequency converting means 12_1 to 12_n. The synthesizers 25_1 to 25_n can also be employed in the embodiments of Figs. 5 and 9.

Fig. 11 illustrates an embodiment according to the first aspect of the present invention. This embodiment differs from the Fig. 1 embodiment in substituting frequency modulating means 31_1 to 31_n for the frequency converting means 12_1 to 12_n. In the frequency modulating means 31_i (where i = 1, 2, ..., n): the frequency of the output signal from a VCO 32_i is divided by a frequency divider 33_i; the phase of the frequency-divided output from the frequency divider 33_i is compared by a phase comparator 35_i with a reference signal from a reference oscillator 34_i; the phase-compared output from the phase comparator 35_i is provided as a control signal to the VCO 32_i; via a low-pass filter 36_i; a signal (carrier) is provided from the VCO 32_i after the frequency of the signal is decided by both the frequency dividing ratio of the frequency divider 33_i and the frequency of the reference signal from the reference oscillator 34_i and is stabilized with the stability of the reference signal; and this carrier is modulated in frequency by the input signal from the input port 22_i and is output from the frequency modulating means 31_i. The frequency dividing ratios of the frequency dividers 33_1 to 33_n or/and the oscillation frequencies of the reference oscillators 34_1 to 34_n are set to different values. Accordingly, individual frequency-modulated signals from the frequency modulating means 31_1 to 31_n belong to different frequency bands, and usually the carrier frequencies are set to be equally-spaced. Interposed between the frequency modulating means 31_1 to 31_n and the power combining

means 16 are the variable attenuators 21_1 to 21_n. This embodiment is identical in construction and operation with the Fig. 5 embodiment except in the points mentioned above.

The frequency converting means 12_1 to 12_n in Figs. 9 and 10 may be replaced with the frequency modulating means 31_1 to 31_n in Fig. 11. For example, as depicted in Fig. 12, the frequency modulating means 31_1 to 31_n in Fig. 11 can be substituted for the frequency converting means 12_1 to 12_n in the Fig. 9 embodiment. The Fig. 12 embodiment employs the common reference frequency oscillation means 26 in place of the reference oscillators 34_1 to 34_n in Fig. 11. The Fig. 11 embodiment may also use the common reference frequency oscillation means 26 as a substitute for the reference oscillators 34_1 to 34_n as shown in Fig. 12. When the frequency modulating means 31_1 to 31_n, typically shown in Figs. 11 and 12, are used, the variable attenuators 21_n are controlled by any one of the schemes described previously with respect of Figs. 6A, 7 and 8.

In the case where the variable attenuators 21_1 to 21_n are separately provided in input paths of the power combining means 16, as shown in Figs. 5 and 11, and the attenuation amounts for the variable attenuators 21_1 to 21_n are all set equal, the influence on the signal is the same as in the case where the multi-carrier signal is attenuated after being multiplexed, In the embodiments of Figs. 9 and 12, when the peak envelope power PEP exceeds the predetermined values, all carrier (modulated) signals are equally limited (or suppressed) -- this is equivalent to intentional distortion of all carrier signals and there are some cases where the information error of each carrier signal arises.

For reducing the envelope power of the multi-carrier signal, there is no need to limit the amplitudes of all the carriers (modulated signals) equally. The envelope power from the power combining means 16 could be reduced to a desired level by such an arrangement as shown in Fig. 13, wherein the modulated signals to be multiplexed, that is, the outputs from the frequency converting means 12_1 to 12_n (or frequency modulating means 31_1 to 31_n) are divided into those to limit the amplitudes and those not to limit, variable attenuators 21_1 to 21_m are provided for limiting the amplitudes of output signals from m frequency converting means 12_1 to 12_m and the output sides of the other frequency converting means 12_{m+1} to 12n are connected directly to the power combining means 16. To perform this, the value m is chosen as described below.

Let the average power per modulated signal be represented by P_0 and the number of modulated signals (or multiplexing number) by n, and suppose that the envelope power of the multi-carrier signal is suppressed when it exceeds k times of the overall average power ($P_a = nP_0$) of the multi-carrier signals. In this instance, the peak envelope power PEP of the (n - m) non-amplitude-limited modulated signals reaches a maximum value of $(n - m)^2P_0$. Since the maximum value is required to be smaller than the predetermined power knP_0, it is necessary to satisfy the following condition:

$$(n - m)^2 P_0 \leq knP_0 \quad (1)$$

From this equation it follows that

$$m \geq n - \sqrt{kn}\,. \quad (2)$$

Of the n modulated signals, m or more modulated signals need only to be controlled for attenuation. In this way, at least m modulated signals whose amplitudes are to be limited are chosen in ascending order of severity of limitations on information errors.

Now, consider the case where the amplitudes of all the carriers are equally limited. Let it be assumed that the power per carrier, after being limited, is xP_0 (where $x < 1$). The overall average power of the multi-carrier signal in this case is xnP_0 and the peak envelope power PEP reaches a maximum of xn^2P_0. Since it is necessary that the peak envelope power be smaller than the predetermined power knP_0,

$$xn^2 P_0 \leq knP_0 \quad (3)$$

Therefore,

$$x \leq k/n. \quad (4)$$

Consider the case where $n = 16$ and $k = 5$, for instance. For dividing the output signals from the frequency converting or modulating means into those to limit the amplitudes and those not to limit, $n - m \leq 8$ is obtained from Eq. (2). That is, the amplitudes of eight carriers of a total of 16 carriers are not limited and the amplitudes of the other remaining carriers are all reduced to zero when their peak envelope power PEP exceeds a predetermined value -- this makes it possible to prevent the peak envelope power of the multi-carrier signal from exceeding a value larger than five times the average power of all the carriers involved. For equally limiting all the carriers, $x \leq 5/16$ is obtained from Eq. (4). By controlling its amplitude when the peak envelope power exceeds a predetermined value, each carrier will lose its power by more than half. In this case, an error can occur in the information of each carrier.

As will be seen from the above, the direct reduction of the envelope power of the multi-carrier signal is equivalent to the equal limitation of the amplitudes of all the carriers; in this instance, there is the possibility of all the carriers having wrong information. In contrast to this, in the case where a variable attenuator is provided for each carrier and the amplitudes of the modulated signals belonging to a specified group are limited, it is possible to preclude the possibility of arising errors in the information of the non-amplitude-limited modulated signals.

When one variable attenuator 21 is provided for the multi-carrier signal as shown in Figs. 9, 10 and 12, there

arise problems that the variable attenuator 21 needs to be a high power-endurable type one since the peak envelope power PEP of the multi-carrier signal is large and that the function of limiting the peak envelope power PEP will be lost if the variable attenuator 21 fails. On the other hand, when the variable attenuator 21_i is provided for each carrier, the attenuator may be a low power-endurable type since the peak envelope power PEP per carrier is not large, and even if one of the variable attenuators 21_i fails, the peak envelope power PEP of the multi-carrier signal can be suppressed; though the function is not enough but to some extent. As will be understood from the afore-mentioned group control, x in the amount of power to be limited, xP_0, is changed with the number of failing variable attenuators and the group control is effected accordingly. It is also possible to employ an arrangement such as indicated by the broken lines in Fig. 13, in which variable attenuators 21_m to 21_n are additionally provided in the channels wherein no amplitude control normally takes place, that is, the variable attenuators 21_i are provided in all the channels; in this instance, the variable attenuators primarily intended for control are selected, but if one or more of them fail, then those of the additionally provided variable attenuators corresponding to the failing ones can be selected as the substitutes therefor. In this way, the influence of failures of the variable attenuators 21_i can be lessened. The above advantage comes solely from the provision of the variable attenuator for each carrier.

Furthermore, in the case where the variable attenuators 21_i are provided in all the channels but attenuation control is carried out for only m attenuators and the amounts of attenuation are set for zero for other remaining n - m variable attenuators, it is possible to adopt a control scheme which; upon completion of each or several control operations for the variable attenuators, changes the group of the m variable attenuators to be controlled so that signal distortions by the amplitude limitation are made as uniform as possible in all the channels. For example, in the case of 16 channels the variable attenuators are divided into a group of those 21_1 to 21_8 and a group of those 21_9 to 21_{16}, and the two groups are alternately controlled.

The changing of the variable attenuators 21_i to be controlled as described above can be made as uniform as possible for all the channels by using such a scheme as shown in Fig. 29.

To begin with, the number m of variable attenuators to be controlled is calculated (S_{24}). Letting the number of modulated waves be represented by n and assuming that the envelope power level is held smaller than k times (set as Ls) of the overall average power of the multi-carrier signal, the number m can be obtained from Eq. (2), that is, $m \geq n - \sqrt{kn}$. Next, a check is made to determine if the condition for controlling the variable attenuators, that is, any of the conditions in step S_2 of Fig. 6A, in step S_{13} of Fig. 7 and in step S_{22} of Fig. 8 is satisfied (S_{25}). If the condition is fulfilled, m different integers $r_1, r_2, ..., r_m$ among I to n are determined by the use of random number generating means (S_{26}). The random number used here is, for instance, a uniform random number in the sense that any integers are equally likely to be selected. With the use of the uniform random number, any variable attenuators 21_i are uniformly selected. Further, since there are well-known methods for generating random numbers having other statistical distributions such as exponential, normal and similar specific distributions by the use of the uniform random number (see, for instance, W. H. Press, B. P. Flannery, S. A. Teukolsky and W. T. Vetterling, "Numerical Recipes in C." Cambridge, New York, 1990, Chapter 7), random numbers other than uniform one can also be employed. In short, any random numbers can be used as long as they serve the purpose of randomly selecting the variable attenuators 21_i.

Next, the amounts of attenuation of the variable attenuators 21_i (where $i = r_1, r_2, ..., r_m$) suffixed with the determined integers $r_1, r_2, ..., r_m$ are set to ∞ [dB] for a predetermined period of time (ΔT) (S_{27}). After the elapsed time ΔT since setting the attenuation to ∞(S_4, S_5), the attenuation amount of the controlled variable attenuators 21_i (where $i = r_1, r_2, ..., r_m$) is reset to 0 [dB] and the process returns to step (S_{25}) for monitoring the envelope power level L (S_{28}).

With this scheme, the variable attenuators that are selected for control are determined by random numbers each time the envelope power level of the multi-carrier signal satisfies the condition for attenuation control. That is, the group of m variable attenuators is changed.

For instance, when n = 16 and k = 5, m ≧ 8, but assume here that m = 8. In this instance, eight integers are selected from among 1 to 16 by using the above-mentioned random numbers. Provided that the eight different integers selected by the random numbers are, for example, 1, 3, 4, 6, 8, 10, 12 and 15, the variable attenuators to be controlled are 21_1, 21_3, 21_4, 21_6, 21_8, 21_{10}, 21_{12} and 21_{15}. Also in this case, the group of variable attenuators to be controlled for attenuation may be changed by the random number generation each time the control for the variable attenuators has been effected a predetermined number of times.

As described above, the modulated signals of all the channels (input routes) need not always be equally attenuated and no attenuation control is required for the modulated signals of some channels; accordingly, it is possible to adopt a control scheme that divides all the channels into a plurality of groups and provides different attenuation amount for each group when the peak envelope power of the multi-carrier signal exceeds a predetermined value. For instance, in the case where the channels are divided into two groups, the attenuation amount for the two groups are selected different about 3 to 5 dB so that the modulated signals, which are required to have a far-lower error rate, are attenuated slightly. In extreme cases, a different attenuation amount may be provided for each channel (input routes). Besides, it is possible to change, when required, the channels in which to greatly attenuate the

modulated signals; hence, in Figs. 5, 9, 10, 11 and 12, the variable attenuators 21_1 to 21_n are each provided in one of the channels and these variable attenuators 21_1 to 21_n are adapted to be separately controllable by the control means 24.

While in the above the envelope power level (PEP) of the multi-carrier signal or the combined output signal from the power combining means 16 is detected by the level detecting means 23 and a check is made to determine if the detected level L is higher than threshold value L_e, it is also possible to employ such a configuration as shown in Fig. 14 wherein the parts corresponding to those in Figs. 5, 9, 10, 11 and 12 are identified by the same reference numerals and wherein the output from the directional coupler 22 is fed not only to the level detecting means 23 but also to average power detecting means 45 to detect the average power P_a of the multi-carrier signal as well, a ratio L/P_a of the peak envelope power PEP detected by the level detecting means 23 or the detected level L to the average power Pa is calculated by the control means 24, then a check is made to see if the ratio L/P_a exceeds a predetermined value A, and if so, predetermined attenuation amount is set in one or more of the variable attenuators 21_1 to 21_n for the predetermined period of time ΔT. In this instance, the variable attenuators may be controlled when the number of times the ratio L/P_a continuously exceeds the predetermined value A reaches the predetermined value M_0 as shown in Fig. 7; or the variable attenuators may be controlled when the L/P_a exceeds the value A for longer than the predetermined period of time T_0 as shown in Fig. 8. Further, it is also possible to omit the variable attenuators 21_1 to 21_n in Fig. 14 and provide a variable attenuator 21 at the output side of the power combining means 16 as indicated by the broken lines.

Next, a description will be given of an embodiment according to the seventh aspect of the present invention which is applied to the multiplexing of FSK modulated signals. Fig. 15 shows the case where m = 2, the parts corresponding to those in Figs. 2 and 3 being identified by the same reference numerals. In the case where m > 2, the device configuration is the same as in the case of m = 2 except that the m-ary FSK modulator 5_i includes m oscillators. In this embodiment, one reference frequency oscillation means 8 is provided and variable phase shifter means 47_i are connected between n (where $n \geq 2$) m-ary FSK modulators 5_i (where i = 1, 2, ..., n) and input ports of respective channels of power combining means 6. The reference frequency signal CLK from the reference frequency oscillating means 8 is provided to the oscillators 2_i and 3_i constructing each m-ary FSK modulator 5_i, and since the oscillation frequencies of the oscillators 2_i and 3_i are synchronized with the reference frequency signal CLK, the oscillator output signals have the same initial phase. The phase of the output signal from each m-ary FSK modulator 5_i is adjusted by the variable phase shifter means 47_i corresponding thereto. The input signal S_i fed via the input port 1_i is branched by branching means 44_i into two routes and input into the m-ary FSK modulator 5_i and a control input port 49_i of control means 48, respectively. The control means 48 sets and adjusts the phase shift amount of each variable phase shifter means 47_i in accordance with a combination of symbols of input signals S_1 to S_n, that is, a combination of n frequencies of the outputs from the n m-ary FSK modulators 5_i (outputs of the oscillators 2_i or 3_i) in synchronization with the timing at which the output frequency of each m-ary FSK modulator 5_i changes. Of course, symbols of the input signals S_1 to S_n are synchronized with one another.

The variable phase shifter means 47_i is a well-known device that can be constructed by a circulator, a variable delay line, or a varactor diode (refer to Miyauchi and Yamamoto, "Microwave Circuits for Communications" pp. 314-321, the Institute of Electronics, Information and Communication Engineers of Japan, 1981), and a commercially available product can be also used. The variable phase shifter means 47_i adjusts the phase of the output signal from the corresponding m-ary FSK modulator 5_i. The control means 48 comprises, as basic circuit components, an A/D converter, a microprocessor, a ROM, a RAM, a D/A converter and a filter, and in accordance with the combination of symbols of the input signals fed to its control input ports 49_i (where i = 1 to n), the control means outputs via its control output ports 50_i control signals V_i which adjust the phase shift amounts of the variable phase shifter means 47_i (where i = 1 to n) to predetermined values. The operation of the control means 48 will be described below.

In each m-ary FSK modulator 5_i, the signal switching means 4_i selects, in accordance with the symbol of the input signal S_i, one of the outputs from the oscillators whose frequencies are predetermined. Figs. 16A and B show, by way of example, the states of the input signal S_i to the m-ary FSK modulator 5_i and the output frequency thereof. In this case, m = 2 and the basic principles are the same also when m > 2. In this way, the signal switching means 4_i switches the oscillation frequency to either one of fi - δf [Hz] and fi + δf [Hz] in accordance with the symbol of the input signal S_i. Here, the m-ary FSK signal is a mere tone signal except at the time of switching oscillation frequencies, and the multiplexed FSK signal can be regarded as a n multitone signal (or multi-frequency signal, i.e. MF signal). The peak envelope power (PEP) of the n multitone signal varies over a wide range in accordance with the combination of initial phases of respective tones. The peak envelope power PEP can be reduced by appropriately adjusting the initial phases of the respective tones of the multitone signal (refer to Narahashi and Nojima, "Peak-factor suppression effects of multi-carrier system with initial-phase assignment method," Spring National Convention Record of the Institute of Electronics, Information and Communication Engineers of Japan, B-388, 1990).

In accordance with the combination of oscillation frequencies which is dependent on the combination of symbols of the input signals to the n m-ary FSK modulators 5_i, the control means 48 sets, as the phase shift

amount for the variable phase shifter means 47_i, an initial phase such that the peak envelope power PEP of the combined signal will not greatly exceed the average power level of the envelope but stay, for example, several-fold. When the multiplexing number of the m-ary FSK signal is n, the number of combinations of symbols is m_n. The control means 48 has a storage means 46 which has stored therein the phase shift amounts precalculated for all symbol combinations; at the timing when the oscillation frequency of the m-ary FSK modulator 5_i changes, that is, at the switching timing when the combination of n frequencies of the respective channels changes, the control means reads out the phase shift amount, corresponding to the combination of symbols of the input signals to the control input ports 49_i (where i = 1 to n), from the storage means 46, and provides via the control output port 50_i a control signal which adjusts the phase shift amount of the variable phase shifter means 47_i on the basis of the read-out value. In other words, the control means adjusts the phase shift amounts of the variable phase shifter means 47i in synchronization with the frequency switching of the output FSK signal from the m-ary FSK modulator 5_i. For instance, if a voltage-controlled phase shifter is used as the variable phase shifter means 47_i, a D/A converter is used to apply a control voltage to the control output port 50_i. In Fig. 16C there is shown an example of the value set for the phase shift amount of the variable phase shifter means 47_i.

With the above-described procedure, it is possible to prevent a substantial increase in the peak envelope power PEP of the multiplexed FSK modulated signal.

While the control operation descried above is to set the phase shift amount of the variable phase shifter 47_i to a predetermined value according to the combinations of symbols of the input signals to the control input ports 49_i of the control means 48, it is also possible to employ a control scheme that the control means 48 sequentially calculates the phase shift amount and sets each variable phase shifter means 47_i to the calculated value. In this case, the control means 48 sequentially calculates the phase shift amount by a microprocessor or the like in accordance with the combination of symbols of the input signals to the control input ports 49_i (where i = 1 to n) and applies a control signal to each variable phase shifter means 47_i via the control output port 50_i.

The sequential calculation of the phase shift amount of the variable phase shifter means 47_i can be done in such a manner as described below. That is, letting the frequencies to be set in the n m-ary FSK modulation means 5_i in accordance with the symbols of the input signals be represented by f_i (where i = 1, ..., n), a complex envelope signal u(t) of a signal produced by multiplexing the output FSK signals of the n m-ary FSK modulating means 5_i is expressed by the following equation:

$$u(t) = \sum_{i=1}^{n} a \exp [j(2\pi f_i t + \theta_i)] \quad (5)$$

where a is the amplitude of each FSK signal and θ_i is the initial phase of an i-th one of the FSK modulated signals. Now, let the maximum value of the multiplexed signal in its one period T, which is determined by the combination $\{\theta_i\}$ of the initial phases, be represented by $A(\theta_1, ..., \theta_n)$.

$$A(\theta_1, ..., \theta_n) = \max |u(t)|, \ t \ [0, T) \quad (6)$$

The peak envelope power PEP of the multiplexed signal is proportional to the square value of $A(\theta_1, ..., \theta_n)$, and hence can be reduced by calculating a combination of initial phases $\{\theta'_i\}$ which reduces $A(\theta_1, ..., \theta_n)$ and then the variable phase shifter means 47_i for each FSK modulated signal is adjusted in accordance with $\{\theta'_i\}$.

A description will be given, with reference to a flowchart of Fig. 30, of an example of a method for calculating the combination of initial phases $\{\theta'_i\}$ which reduces $A(\theta_1, ..., \theta_n)$.

$A(\theta_1, ..., \theta_n)$ is calculated for each of a plurality (M_0) of predetermined combinations of initial phase and one of the combinations of initial phases which reduces $A(\theta_1, ..., \theta_n)$ is output as $\{\theta'_i\}$. The M_0 combinations of initial phases $\{\theta_i\}$ are generated, for example, by changing the initial phase θ_i (where i = 1, ..., n) of the FSK modulated signals for each minimum phase step ($\Delta\theta$). Setting $\Delta\theta = 2\pi/K$ (where K is an integer equal to or greater than 2). $M_0 = K^n$ in case of taking into account all the combinations of initial phases.

In Fig. 30, the frequency f_i of the FSK signal from each m-ary FSK modulation means 5_i is set according to the input signal (symbol) thereto (S_1), and the variable M representing the number of times the calculation has been conducted is initialized to zero and variable A_{min} representing the minimum one of the calculated values $A(\theta_1, ..., \theta_n)$ is initialized to na (the maximum value of $A(\theta_1, ..., \theta_n)$)($S_2$). The M_0 combinations of initial phases $\{\theta_i\}$ are each set in a predetermined sequential order (S_3), then $A(\theta_1, ..., \theta_n)$ is calculated for that combination of initial phases $\{\theta_i\}$ (S_4) and a check is made to see if the calculated $A(\theta_1, ..., \theta_n)$ is smaller than a predetermined value A_{th} (S_5). If so, the combination of initial phase $\{\theta_i\}$ at that time is output as the combination of initial phases $\{\theta'_i\}$ which reduces $A(\theta_1, ..., \theta_n)$ (S_6), thereafter being set in each variable phase shifter means 17_i (S_7).

If it is found in step S_5 that $A(\theta_1, ..., \theta_n)$ is not smaller than the predetermined value A_{th}, then a check is made to determine whether $A(\theta_1, ..., \theta_n)$ is smaller than the variable A_{min} (S_8); if smaller, $A(\theta_1, ..., \theta_n)$ is updated with the value A_{min}, then the combination of initial phase $\{\theta_i\}$ is output as the combination of initial phases $\{\theta'_i\}$ (S_9) and M is incremented by one (S_{10}).

If it is found in step S_8 that $A(\theta_1, ..., \theta_n)$ is not smaller than the value A_{min}, then the process precedes

to step S_{10}. After the variable M is incremented by one, a check is made to see if the variable M is equal to M_0 (S_{11}); if not, the process returns to step S_3, wherein the same calculations and processes as described above are carried out using the next combination of initial phases $\{\theta_i\}$. If $M = M_0$ in step S_{11}, then the combination of initial phases $\{\theta'_i\}$ at that time is set in each variable phase shifter means 17_i (S_7).

In the above, steps S_5 and S_6 may be omitted. In such an instance, from among the M_0 predetermined combinations of initial phases, $\{\theta_i\}$ that provides the minimum value of $A(\theta_1, ..., \theta_n)$ is selected and used as the combination of initial phases $\{\theta'_i\}$ and the phase shift amount of each variable shifter means 47_i is set accordingly.

In short, since the peak value of the multiplexed signal needs only to be not more than a allowable value, for example, equal to or less than 4 to 5 times the average power of the multiplexed signal itself, it is not always necessary to calculate the combination of initial phases $\{\theta'_i\}$ that minimizes the peak value of the multiplexed signal, on the basis of the combination of input symbols; the computational complexity could be reduced by using the value A_{th} in step S_5 as the above-mentioned allowable value. From such a viewpoint, it will be understood that the number of calculations involved could be decreased by setting the initial phase θ_i (where $i = 1, ..., n$) as random values which are uniformly distributed in $[0, 2\pi)$ in step S_3, instead of calculating $A(\theta_1, ..., \theta_n)$ for all the combination of phases that are generated by changing the initial phases $\{\theta_i\}$ with the minimum phase step $\Delta\theta = 2\pi/K$ in $[0, 2\pi)$ and by setting the value M_0 to a number smaller than K^n.

In Fig. 17 there is shown an example wherein each m-ary FSK modulator 5_i in the Fig. 15 embodiment is constructed by the PLL frequency synthesizer in Fig. 3, the parts corresponding to those in Figs. 3 and 15 being identified by the same reference numerals.

Fig. 18 illustrates an example wherein the m-ary FSK modulator 5_i and the variable phase shifter means 47_i in Fig. 15 are constructed by a direct digital frequency synthesizer (DDS) 51_i. In Fig. 19 there is shown an example of the basic configuration of the DDS 51_i. In the DDS 51_i: the input signal S_i provided via the branching means 44_i is converted by data converting means 52_i into an oscillation frequency data value; the oscillation frequency data value from the data converting means 52_i is stored in a frequency register 53_i; the oscillation frequency data value in the frequency register 53_i is accumulated by an accumulator 55_i; the accumulated value is added by an adder 56_i to an initial phase data value from a phase register 54_i; and the added data value is used to read out data from a waveform ROM 57_i; and the read-out data is converted by and D/A converter 58_i into an analog signal for output. The direct digital frequency synthesizer DDS is supplied with the reference frequency signal CLK, by which the accumulating operation of the accumulator 55_i and the read-put operation of the waveform ROM 57_i are conducted, the oscillation frequency data value is switched in accordance with the input signal S_i to set the frequency of the FSK signal to be output, and data corresponding to the control signal V_i is set in the phase register 54_i to thereby set the phases of the FSK signal to be output from the DDS 51_i. The Fig. 18 embodiment is identical in construction with the Fig. 15 embodiment except the above.

It is also possible to employ relatively low-speed and low-cost variable phase shifter means 47_i and control means 48 through utilization of such an arrangement as shown in Fig. 20, wherein delay means 59_i is connected in series between each branching means 44_i and the DDS 51_i (or m-ary FSK modulator 5_i) so that the inputting of the input signal S_i to the DDS 51_i (or m-ary FSK modulator 5_i) is delayed behind the input to the control means 48.

As shown in Fig. 21, frequency converting means 63 may be provided at the output side of the power combining means 6 so that the multiplexed signal from the power combining means 6 is converted by the frequency converting means 63 to a signal of a higher frequency band. The frequency converting means 63 is made up of a local oscillator 60, a mixer 61 for multiplying output signals from the local oscillator 60 and the power combining means 6, and band-pass filter means 62 provided at the output side of the mixer 61 to remove signals of unnecessary frequency bands resulting from the multiplication.

In Fig. 22, frequency converting means 67_i is provided in the output path of each DDS 51_i, and the outputs form the direct digital frequency synthesizers 51_1 to 51_n are converted into high-frequency signals of different frequency bands, thereafter being fed to the power combining means 6. In this instance, the center frequency (the carrier frequency) of the output from the DDS 51_i or m-ary FSK modulator 5_i in each channel can be set to a relatively low fixed value -- this facilitates the designing of these circuits including the variable phase shifter means and permits the use of inexpensive parts. In the frequency converting means 67_i, the output signal from a frequency synthesizer 64_i, which uses the output from the reference frequency oscillating means 8 as a reference frequency signal, is multiplied by the output signal from the DDS 51_i in a mixer 65_i, and the multiplied output is fed to the power combining means via band-pass filter means 66_i wherein signals of unnecessary frequency bands resulting from the multiplication are eliminated.

Fig. 23 illustrates an example in which there is provided at the output side of each DDS 51_i band-pass filter means 68_i which permits the passage therethrough of its output FSK modulated signal and outputs from such band-pass filter means 68_i are combined by the power combining means 6. With the afore-mentioned m-ary FSK modulated signal generation method by switching the output signals from a plurality of oscillating means (Fig. 15), the phase of the m-ary FSK modulated signal usually becomes discontinuous at the time of

switching the oscillation frequency. Also with the method employing the PLL frequency synthesizers (Fig. 17), similar phase discontinuity occurs when a sharp phase shift is done by the variable phase shifter means 47_i. This causes spreading of the spectrum of the output m-ary FSK modulated signal. The band-pass filter means 68_i is used to suppress the spreading of the spectrum. The power-combined output of the modulated signals, with the spreading of their spectra thus suppressed in the respective channels, may be converted by the frequency converting means 63 to a high-frequency band signal as depicted in Fig. 21. That is to say, the configurations shown in Figs. 21 and 23 may preferably be combined.

As shown in Fig. 24, low-pass filter means 69_i may be provided between each DDS 51_i and the frequency converting means 67_i in Fig. 22. The low-pass filter means 69_i is intended to suppress the spreading of the spectrum as is the case with the band-pass filter means 68_i in the Fig. 23 embodiment.

In Fig. 21, the same effect could be also produced by connecting the low-pass filter means 69_i to the input side of the power combining means 6.

As depicted in Fig. 25, control signal processing means 70 is provided in the control means 48 in Fig. 17, by which the control signal for setting the phase shift amount of the variable phase shifter means 47_i is so processed as to suppress the spreading of the spectrum of the output m-ary FSK modulated signal, and then thus processed control signal is provided to the control output port 50_i. For example, if a voltage-controlled phase shifter is used as the variable phase shifter means 47_i, phase shift amount data, read out in accordance with the combination of symbols of the input signals to each control input port 49_i, is converted by a D/A converter to an analog voltage, which is provided to the control output port 50_i after being processed by a low-pass filter so that the phase shift amount of the variable phase shifter means 50_i does not vary stepwise. In Fig. 16D there is shown, comparing with an example which performs no filter processing of the control voltage (Fig. 16C), a waveform of the phase control signal V_i which is processed to inhibit the spreading of the spectrum of the m-ary FSK modulated signal. If the m-ary FSK modulated signal multiplexer is constructed by using the DDS 51_i, the phase of the m-ary FSK modulated signal from the DDS 51_i could be made continuous by processing the data from the control output port 50_i to the phase register 54_i (Fig. 19) with the control signal processing means 70. Incidentally, the same effect can be obtained regardless of whether the control signal processing means 70 is disposed inside or outside of the control means 48.

In the above embodiments employing the variable phase shifter means 47_i, their positions are not limited specifically to those shown; they may be disposed at any other position as long as the phase of each m-ary FSK modulated signal can be adjusted. Fig. 26 illustrates an embodiment in which the variable phase shifter means 47_i is provided in the path over which the reference frequency signal from the reference frequency oscillating means 8 is fed to each m-ary FSK modulator 5_i. This embodiment is identical in construction with the Fig. 25 embodiment except the above. Also in this case, the phase of each m-ary FSK modulated signal can be adjusted by adjusting the phase shift amount of the variable phase shifter 47_i because the output signal from the m-ary FSK modulator 5_i is synchronized with the reference signal CLK from the reference frequency oscillating means 8.

Incidentally, the part indicated by the DDS 51_i in the above embodiments may be replaced with such an m-ary FSK modulator 5_i and variable phase shifter means 47_i as shown in Fig. 17.

While as shown in Figs. 15 to 26 the phase shift amount in each channel is controlled in accordance with the combination of symbols of input signals to prevent a substantial increase in the peak envelope power of the multiplexed m-ary FSK modulated signal, the configuration therefor can also be used in combination with the configuration that suppresses the peak envelope power by providing the attenuation as described previously with respect to Figs. 5 to 12. The basic configurations are shown in Figs. 27 to 28, in which the parts corresponding to those in Figs. 5 to 26 are identified by the same reference numerals. In Fig. 27 the variable attenuators 21_1 to 21_n are connected in series to the output sides of the m-ary FSK modulators 5_1 to 5_n, respectively, the control of the variable attenuators 22_1 to 21_n based upon the envelope power level detected by the level detecting means 6 and the control for the variable phase shifter means 47_1 to 47_n are effected by common control means 81. In Fig. 28 the variable attenuating means 21 is connected in series to the output side of the power combining means 6 (or 16), the envelope power level of the output multiplexed signal from the power combining means 6 is detected by the level detecting means 23. The variable attenuating means 21 and the variable phase shifter means 47_1 to 47_n are placed under the control of the control means 81. In Figs. 27 and 28 it is also possible to construct the m-ary FSK modulator 5_i and the variable phase shifter means 47_i by the DDS 51_i as mentioned previously and convert the signal to a high-frequency band at the input or output side of the power combining means 6; furthermore, the modifications and variations described previously in respect of Figs. 15 to 26 can be applied to the embodiments of Figs. 27 and 28.

As described above, according to the first to sixth aspects of the present invention, it is possible to suppress a large peak envelope power level of the multiplexed signal. In addition, since the signal is attenuated for only a predetermined period of time, that is, since the signal is attenuated only to such an extent as the width of an instantaneous peak value, the information contained in the modulated signal only undergoes an instantaneous distortion, and hence is not seriously affected.

In the case where attenuation is provided only when the number of times or the period of time the envelope power level continuously exceeds a predetermined level reaches a predetermined value, no attenuation control is effected when the amplifier at the preceding stage will not be greatly affected even if the envelope power level is higher than the predetermined level. Hence, the information contained in the modulated signal is less distorted accordingly.

In case of the device configuration wherein modulated signals are divided into those to be attenuated and those not, the peak of the envelope power is suppressed but some of the modulated signals (channels) are entirely free from the influence of the suppression on the channels where the requirement about the error rate is severe can be lessened as compared with the influence of uniform attenuation in all channels.

According to the seventh aspect of the present invention, the peak envelope power level of the multiplexed signal can be sufficiently lowered by controlling the phase shift amount of each m-ary FSK modulated signal in synchronization with a change in the symbol of the input and by effecting the control for each channel in accordance with the symbol state of each input signal. Furthermore, the application of the first or second aspect to the ninth one of the present invention ensures sufficient suppression of the peak envelope power of the multiplexed signal.

Claims

1. A signal multiplexer wherein modulated signals of different frequency bands fed via n input channels are combined by power combining means to a multiplexed signal for output to an output port, n being an integer equal to or greater than 2, said signal multiplexer comprising:

   m' (where m' ≦ n) variable attenuating means connected in series to an input port of said power combining means in association with m' ones of said n input channels;

   envelope power level detecting means for detecting the envelope power level of said multiplexed signal; and

   control means for setting predetermined attenuation amount in m (where m ≦ m') ones of said variable attenuating means for a predetermined period of time when said detected envelope power level exceeds a predetermined level.

2. The signal multiplexer of claim 1, wherein said predetermined attenuation amount set in said attenuating means is the same.

3. The signal multiplexer of claim 2, wherein said m is n, said predetermined level is k times the average power of said multiplexed signal, k being substantially in the range of 1 to 10, and said predetermined attenuation amount is equal to or more than 10 log (k/n) [dB].

4. The signal multiplexer of claim 1, wherein said predetermined level is k times the average power of said multiplexed signal, k being substantially in the range of 1 to 10, m < n, (n - m) is set to a value equal to or smaller than the maximum integer not greater than $\sqrt{kn}$, attenuation amount of said (n - m) variable attenuating means in which said predetermined attenuation amount is not set is set to zero, and said predetermined attenuation amount of m variable attenuating means other than said (n - m) ones is set to infinity.

5. The signal multiplexer of claim 1, wherein m < n, and further comprising:

   switching means whereby said variable attenuating means in which said predetermined attenuation amount is set and said variable attenuating means in which said predetermined attenuation amount is not set are switched each time when said attenuation amount is set once or more times.

6. The signal multiplexer of claim 5, wherein said switching means is means for randomly selecting said m variable attenuating means among said n variable attenuating means.

7. The signal multiplexer of claim 5, wherein said predetermined level is k times the average power of said multiplexed signal, k being substantially in the range of 1 to 10, (n - m) is set to a value equal to or smaller than the maximum integer not greater than $\sqrt{kn}$, attenuation amount of said (n - m) variable attenuating means in which said predetermined attenuation amount is not set is set to zero, and said predetermined attenuation amount of m variable attenuating means other than said (n - m) ones is set to infinity.

8. The signal multiplexer of claim 1, wherein some of said predetermined attenuation amounts are different from others in said variable attenuating means.

9. The signal multiplexer of claim 1, wherein said predetermined level is k times the average power of said multiplexed signal, k being substantially in the range of 1 to 10.

10. A signal multiplexer wherein modulated signals of different frequency bands fed via n input channels are combined by power combining means to a multiplexed signal for output to an output port, n being an integer equal to or greater than 2, said signal multiplexer comprising:

    variable attenuating means connected in series between said power combining means and said output port;

envelope power level detecting means for detecting the envelope power level of said multiplexed signal; and

control means for setting predetermined attenuation amount in said variable attenuating means for a predetermined period of time when said detected envelope power level exceeds a predetermined level.

11. The signal multiplexer of claim 10, wherein said predetermined level is k times the average power of said multiplexed signal, k being substantially in the range of 1 to 10.

12. The signal multiplexer of any one of claims 1 to 11, wherein said predetermined period of time is about $T_p = 1/\Delta F_0$ (sec), ΔF_0 [Hz] being the bandwidth of said multiplexed signal.

13. The signal multiplexer of any one of claims 1 to 11, wherein said control means is means for setting said attenuation amount when said detected envelope power level continuously exceeds said predetermined level more than a predetermined number of times.

14. The signal multiplexer of claim 13, wherein said predetermined period of time is about $T_p = 1/\Delta F_0$ (sec), ΔF_0 [Hz] being the bandwidth of said multiplexed signal.

15. The signal multiplexer of any one of claims 1 to 11, wherein said control means is means for setting said attenuation amount when said detected envelope power level continuously exceeds said predetermined level for longer than a predetermined period of time.

16. The signal multiplexer of claim 15, wherein said predetermined period of time is about $T_p = 1/\Delta F_0$ (sec), ΔF_0 [Hz] being the bandwidth of said multiplexed signal.

17. A signal multiplexer wherein modulated signals of different frequency bands fed via n input channels are combined by power combining means to a multiplexed signal for output to an output port, n being an integer equal to or greater than 2 comprising:

n variable attenuating means connected in series to input ports of said power combining means in respective input channels;

envelope power detecting means for detecting the envelope power level of said multiplexed signal;

average power detecting means for detecting the average power of said multiplexed signal; and

control means for setting predetermined attenuation amount in m (where $m \leq n$) ones of said variable attenuating means for a predetermined period of time when the ratio of said detected envelope power level to said detected average power exceeds a predetermined value.

18. A signal multiplexer wherein modulated signals of different frequency bands fed via n input channels are combined by power combining means to a multiplexed signal for output to an output port, n being an integer equal to or greater than 2, said signal multiplexer comprising:

variable attenuating means connected in series between said power combining means and said output port;

envelope power level detecting means for detecting the envelope power level of said multiplexed signal;

average power detecting means for detecting the average power of said multiplexed signal; and

control means for setting predetermined attenuation amount in said variable attenuating means for a predetermined period of time when the ratio of said detected envelope power level to said detected average power exceeds a predetermined value.

19. A signal multiplexing method wherein modulated signals of different frequencies fed via n input channels are combined to a multiplexed signal for output, n being an integer equal to or greater than 2, said method comprising the steps of:

detecting the envelope power level of said multiplexed signal;

comparing said detected envelope power level with a predetermined level; and

providing predetermined attenuation amount to m ($m \leq n$) ones of said n modulated signal for a predetermined period of time when said detected envelope power level is higher than said predetermined level.

20. The signal multiplexing method of claim 19, wherein said m is smaller than n, and further comprising a step of changing (or updating) the combination of m modulated signal to be attenuated each time when said predetermined attenuation amount is provided.

21. A signal multiplexing method wherein modulated signals of different frequencies fed via n input channels are combined to a multiplexed signal for output, n being an integer equal to or greater than 2, said method comprising the steps of:

detecting the envelope power level of said multiplexed signal;

comparing said detected envelope power level with a predetermined level; and

providing predetermined attenuation amount

to said multiplexed signal for a predetermined period of time when said detected envelope power level is higher than said predetermined level.

22. The signal multiplexing method of any one of claims 19 to 21, wherein said step of providing predetermined attenuation amount comprises the steps of:

incrementing a count value by one when said detected envelope power level is higher than said predetermined level; making a check to determine if said incremented count value reaches a predetermined value and, if so, causing the provision of said predetermined attenuation amount to be executed and, if not, returning to said envelope power level detecting step; and resetting said count value to zero and returning to said envelope power level detecting step if said detected envelope power level is lower than said predetermined level.

23. The signal multiplexing method of any one of claims 19 to 21, wherein said step of providing predetermined attenuation amount comprises the steps of:

beginning the counting of time if said detected envelope power level is higher than said predetermined level;

making a check to determine if said time counted reaches a predetermined value and, if so, causing the provision of said predetermined attenuation amount to be executed and, if not, returning to said envelope power level detecting step; and

resetting said time count value to zero and returning to said envelope power level detecting step if said detected envelope power level is lower than said predetermined level.

24. A signal multiplexer wherein n (n channels) m-ary FSK modulating means (where m and n are integers each equal to or greater than 2) for shifting their output frequencies in accordance with the symbols of input signals thereto are supplied with a common reference frequency signal from reference frequency oscillating means as the reference for the frequency of the output signal from each of said m-ary FSK modulating means and said output signals are combined by power combining means for output, said signal multiplexer comprising:

variable phase shifter means for shifting the phases of the output modulated signals from said m-ary FSK modulating means; and

control means for setting the phase shift amounts of said phase shifter means to reduce the peak envelop power of the output from said power combining means, in accordance with a combination of symbols of said n input signals in synchronization with the timing for said m-ary FSK modulating means to switch their output frequencies according to the input signals thereto.

25. The signal multiplexer of claim 24, wherein said m-ary FSK modulating means each comprise m oscillators of different oscillation frequencies, and signal switching means for selectively outputting the oscillation signal from one of said m oscillators in accordance with the symbol of said input signal, and said variable phase shifter means are each connected in series to the output side of one of said m-ary FSK modulating means.

26. The signal multiplexer of claim 24, wherein said m-ary FSK modulating means each comprise m oscillators of different oscillation frequencies, and signal switching means for selectively outputting the oscillation signal from one of said m oscillators in accordance with the symbol of said input signal, and said variable phase shifter means are each connected in series to an input port of one of said m-ary FSK modulating means to which said reference frequency signal is input.

27. The signal multiplexer of claim 25, wherein said m-ary FSK modulating means are each constructed by a PLL frequency synthesizer, and said variable phase shifter means are each connected in series to the output side of one of said m-ary FSK modulating means.

28. The signal multiplexer of claim 26, wherein said m-ary FSK modulating means are each constructed by a PLL frequency synthesizer; and said variable phase shifter means are each connected in series to an input port of one of said m-ary FSK modulating means to which said reference frequency signal is input.

29. The signal multiplexer of claim 24, wherein said m-ary FSK modulating means and said variable phase shifter means in each of said channels are constructed by a direct digital frequency synthesizer (DDS).

30. The signal multiplexer of any one of claims 24 to 29, further comprising:

n branching means each for branching said input signal in said each channel for supply to both one of said m-ary FSK modulating means and said control means; and

delay means provided in a path of said input signal between said each branching means and said m-ary FSK modulating means corresponding thereto.

31. The signal multiplexer of any one of claims 24 to 29, wherein frequency converting means is provided at the output side of said power combining means to convert said combined signal therefrom to a high-frequency signal.

32. The signal multiplexer of claim 31, wherein low-pass filter means is provided at the input side of said power combining means in each channel to limit the bandwidth of said modulated signal.

33. The signal multiplexer of any one of claims 24 to 29, wherein frequency converting means is provided at the input side of said power combining means in each channel to convert said modulated signal thereto to a high-frequency signal.

34. The signal multiplexer of claim 33, wherein low-pass filter means is provided at the input side of each of said frequency converting means to limit the bandwidth of said modulated signal.

35. The signal multiplexer of any one of claims 24 to 29, wherein band-pass filter means is provided at the input side of said power combining means in each channel to limit the bandwidth of said modulated signal.

36. The signal multiplexer of any one of claims 24 to 29, wherein said control means has storage means for phase shift amounts to be set in said variable phase shifter means in accordance with the combination of symbols of said n input signals.

37. The signal multiplexer of any one of claims 24 to 29, wherein said control means has means for sequentially calculating the phase shift amounts to be set in said variable phase shifter means in accordance with the combination of symbols of said input signals.

38. The signal multiplexer of any one of claims 24 to 29, wherein said control means has control signal processing means for processing a control signal to control the phase shift amounts of said variable phase shifter means so that the phase of each FSK modulated signal to be input into said power combining means is continuous.

39. The signal multiplexer of any one of claims 24 to 29, further comprising:

n variable attenuating means each connected in series to the output side of one of said m-ary FSK modulating means;

means for detecting the envelope power level of the combined output signal from said power combining means; and

control means for setting predetermined attenuation amount in p ($p \leq n$) ones of said variable attenuating means for a predetermined period of time when said detected envelope power level exceeds a predetermined value.

40. The signal multiplexer of any one of claims 24 to 29, further comprising:

variable attenuating means connected in series to the output side of said power combining means;

means for detecting the envelope power level of the combined output signal from said power combining means; and

control means for setting predetermined attenuation amount in said variable attenuating means for a predetermined period of time when said detected envelope power level exceeds a predetermined value.

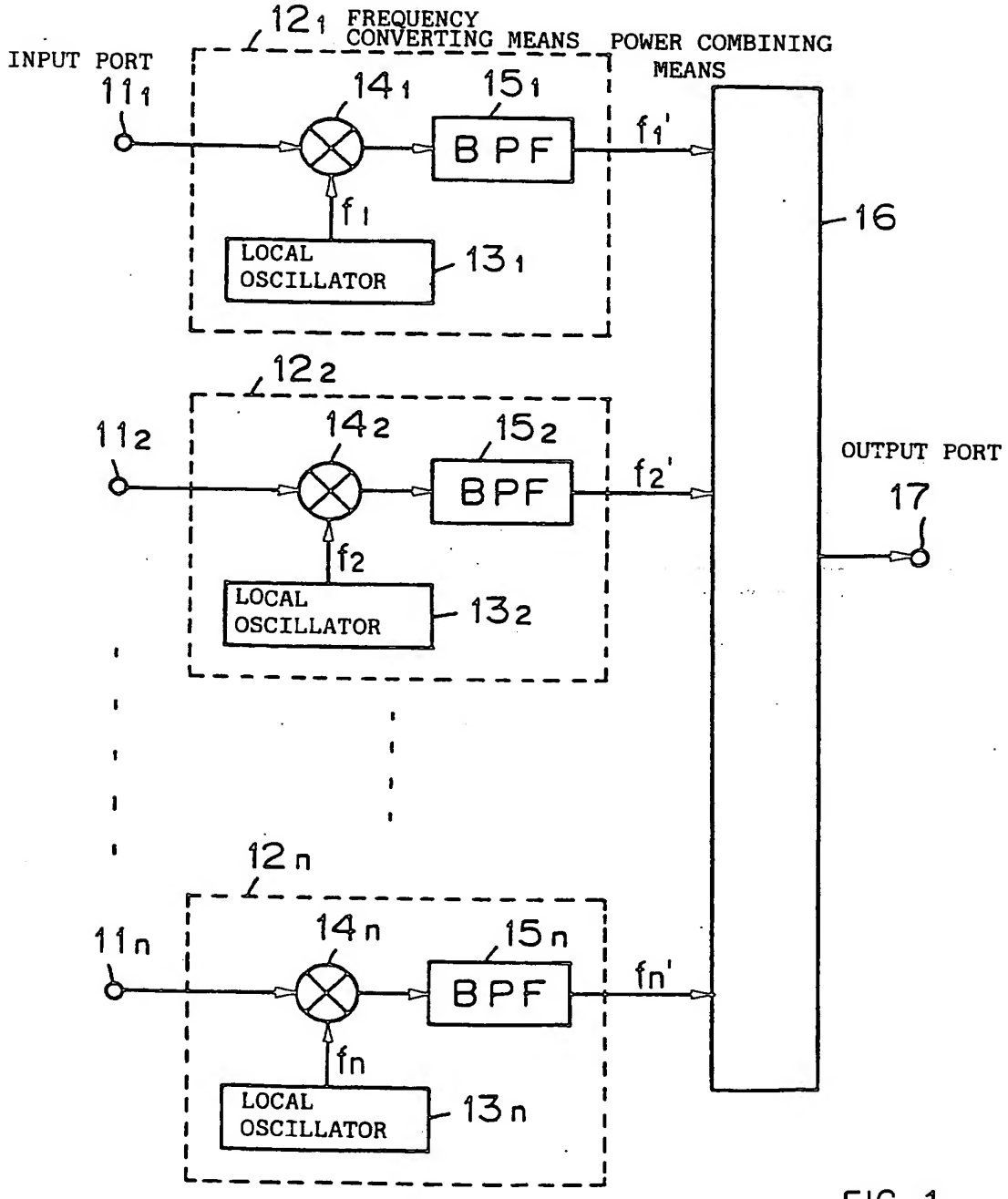

12 1 FREQUENCY CONVERTING MEANS
POWER COMBINING MEANS
INPUT PORT
11 1
14 1
15 1
BPF
f1'
f1
LOCAL OSCILLATOR
13 1
16
12 2
11 2
14 2
15 2
BPF
f2'
OUTPUT PORT
17
f2
LOCAL OSCILLATOR
13 2
12 n
11 n
14 n
15 n
BPF
fn'
fn
LOCAL OSCILLATOR
13 n

FIG. 1

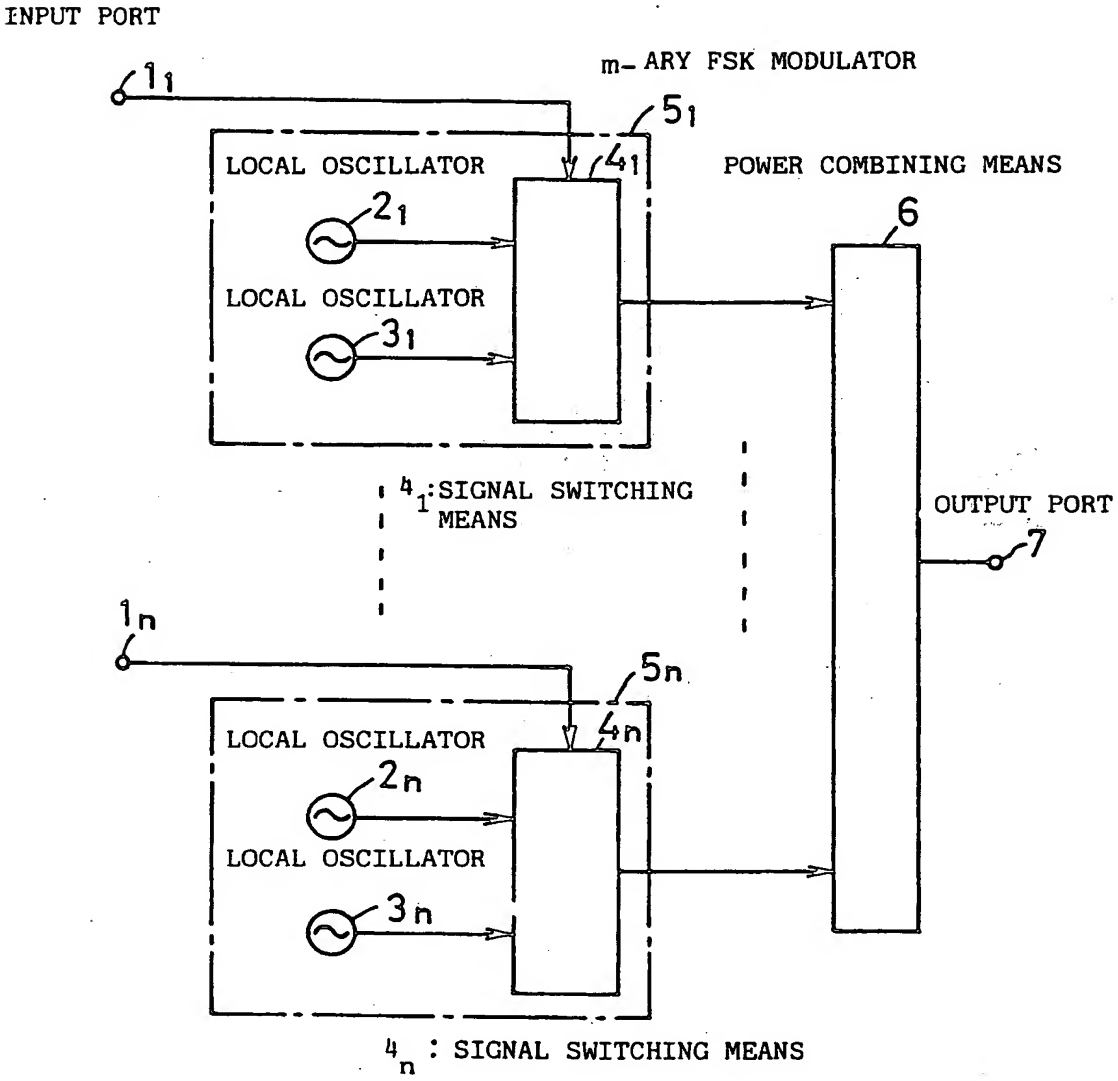


FIG.2

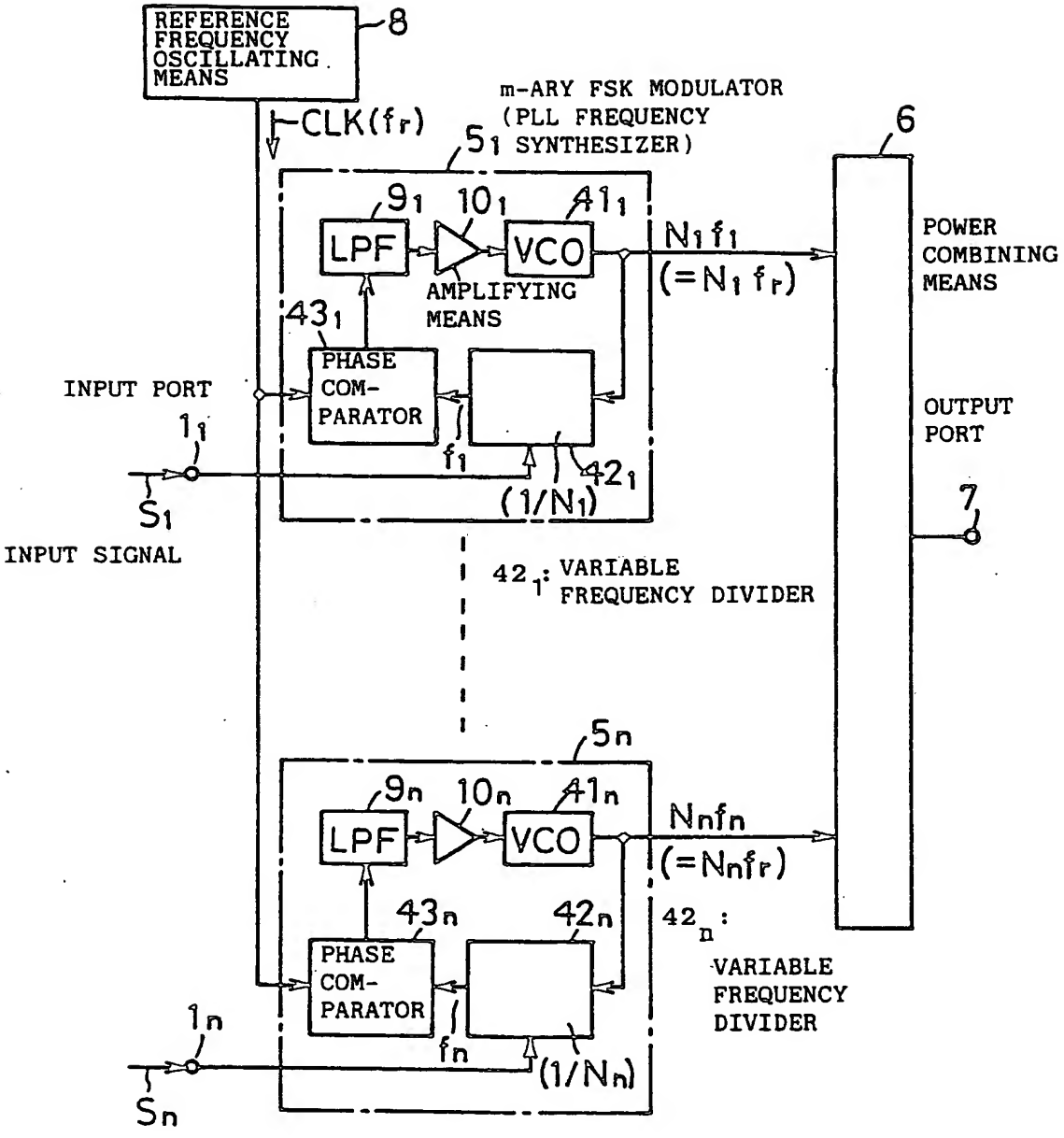

REFERENCE FREQUENCY OSCILLATING MEANS
8
CLK(fr)
m-ARY FSK MODULATOR (PLL FREQUENCY SYNTHESIZER)
51
91
101
41 1
LPF
VCO
AMPLIFYING MEANS
N1f1
(=N1fr)
6
POWER COMBINING MEANS
431
PHASE COM-PARATOR
INPUT PORT
11
f1
421
(1/N1)
OUTPUT PORT
7
S1
INPUT SIGNAL
421: VARIABLE FREQUENCY DIVIDER
5n
9n
10n
41n
LPF
VCO
Nnfn
(=Nnfr)
43n
42n
PHASE COM-PARATOR
421: VARIABLE FREQUENCY DIVIDER
1n
fn
(1/Nn)
Sn

FIG.3

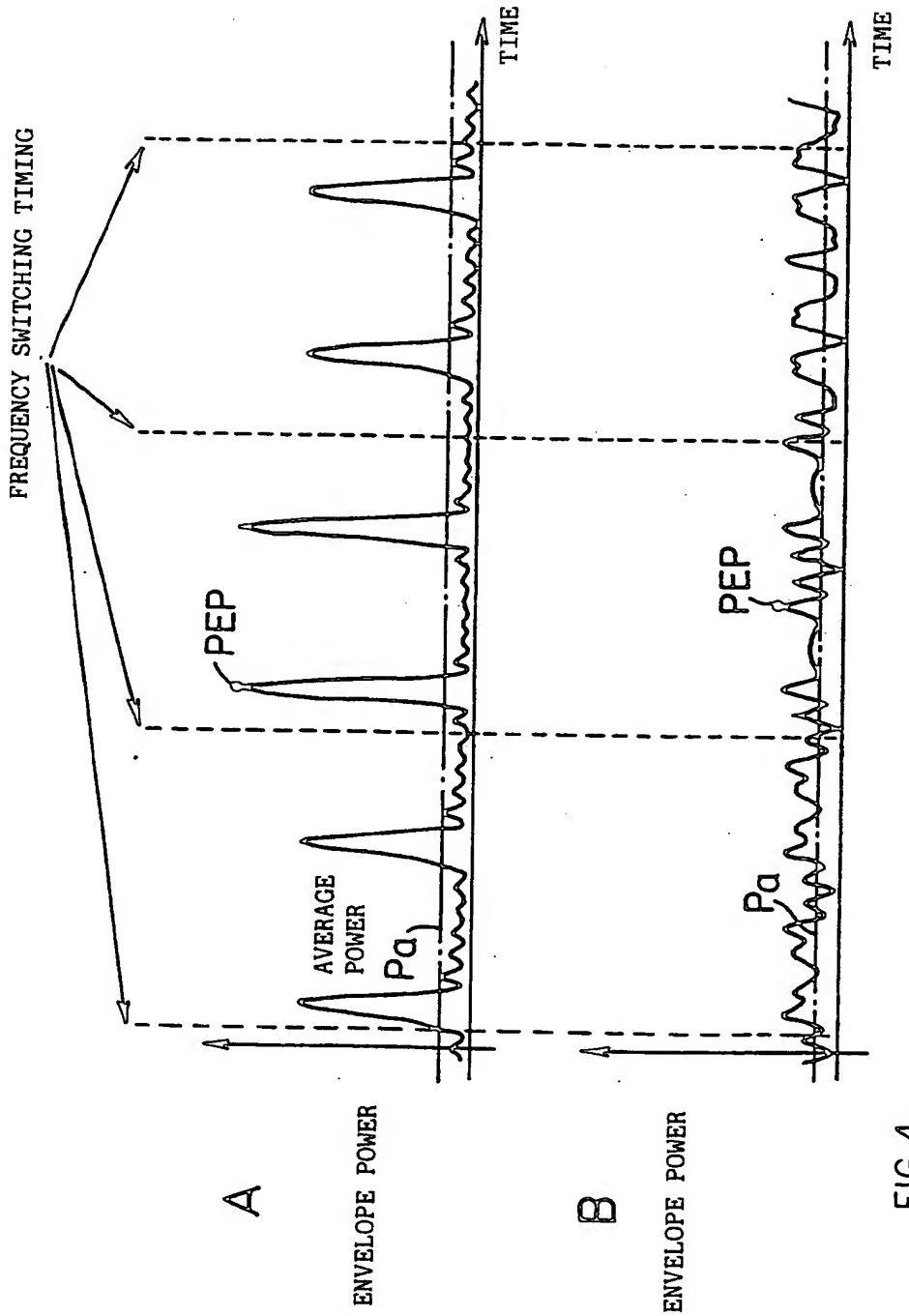


FIG.4

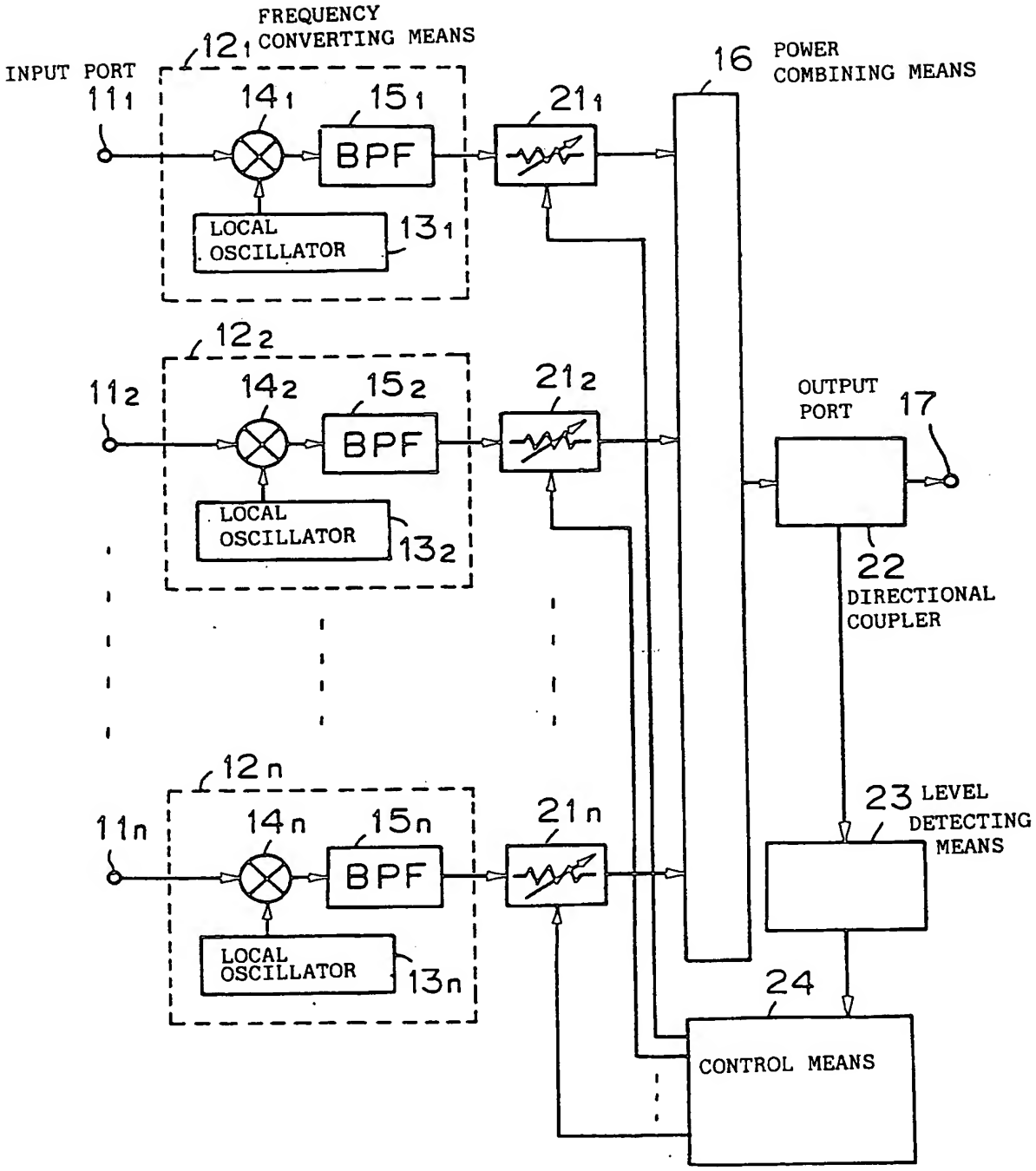
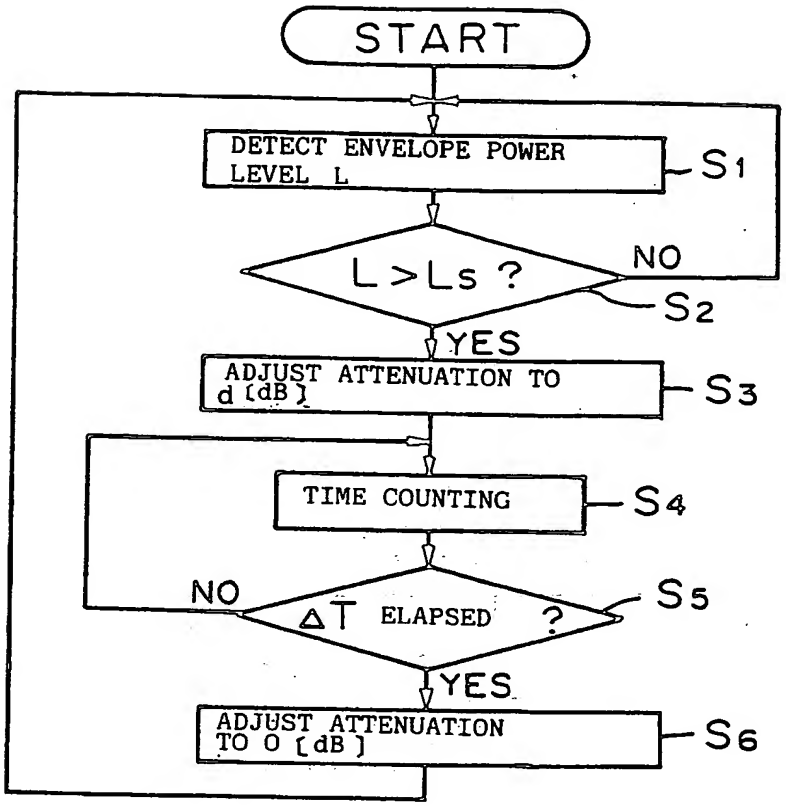

FREQUENCY CONVERTING MEANS
12 1
INPUT PORT
11 1
14 1
15 1
BPF
21 1
16
POWER COMBINING MEANS
LOCAL OSCILLATOR
13 1
12 2
11 2
14 2
15 2
BPF
21 2
OUTPUT PORT
17
LOCAL OSCILLATOR
13 2
22
DIRECTIONAL COUPLER
12 n
11 n
14 n
15 n
BPF
21 n
23
LEVEL DETECTING MEANS
LOCAL OSCILLATOR
13 n
24
CONTROL MEANS

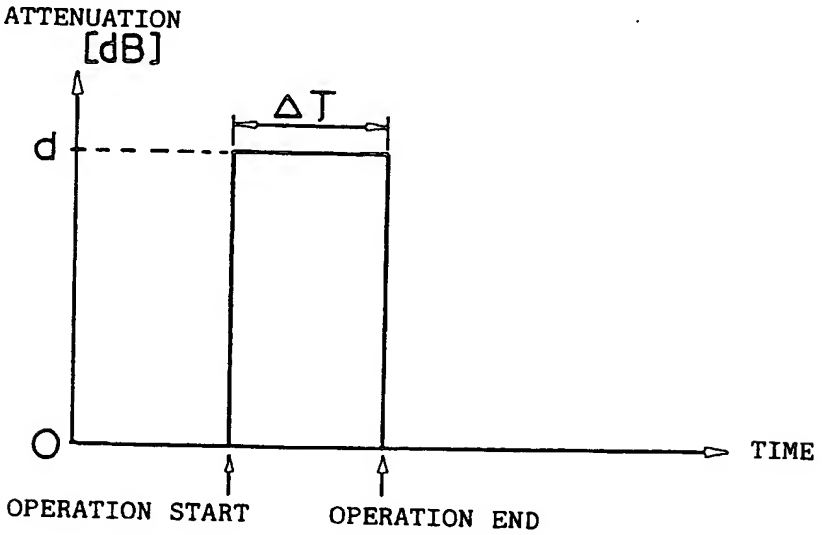
FIG.5

FIG. 6

A



B



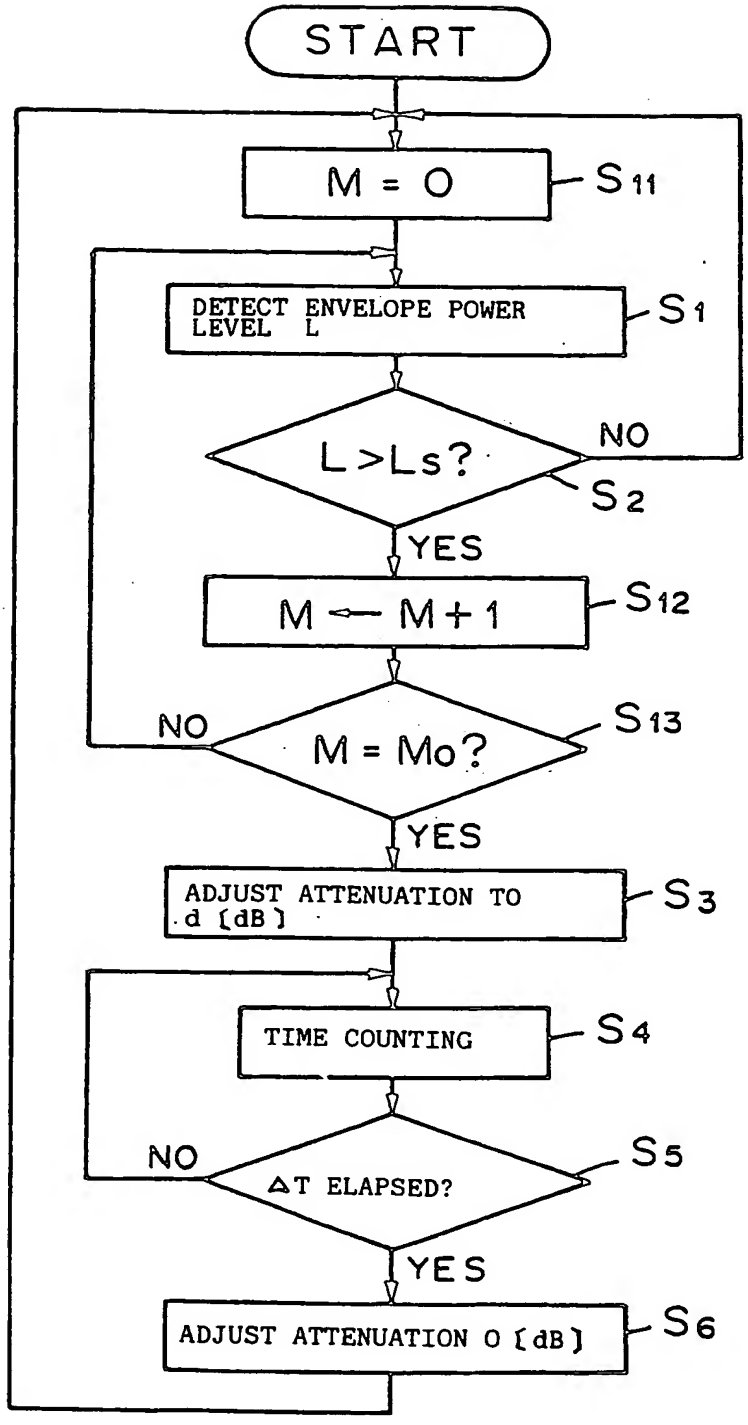

START
M = O
S11
DETECT ENVELOPE POWER LEVEL L
S1
L>Ls?
NO
S2
YES
M ← M+1
S12
NO
M = Mo?
S13
YES
ADJUST ATTENUATION TO d [dB]
S3
TIME COUNTING
S4
NO
ΔT ELAPSED?
S5
YES
ADJUST ATTENUATION O [dB]
S6

FIG. 7

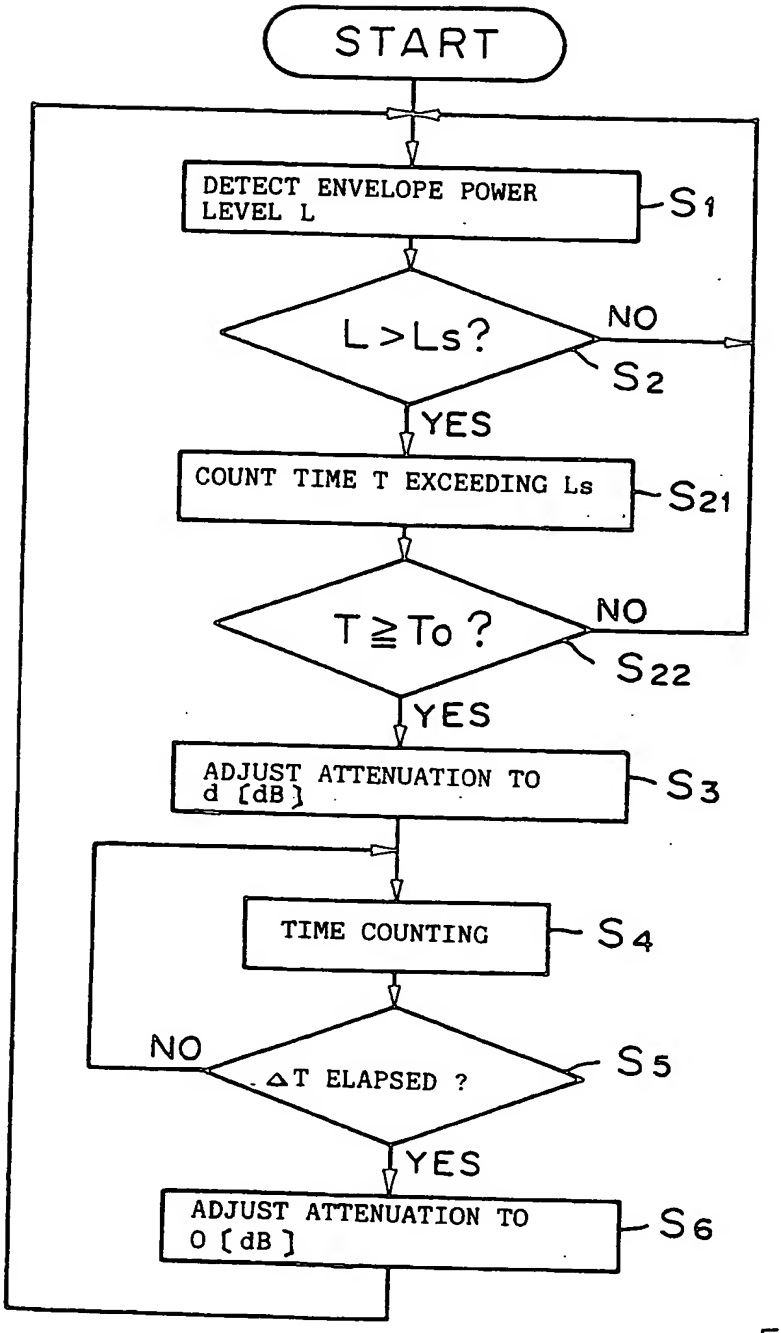


FIG. 8

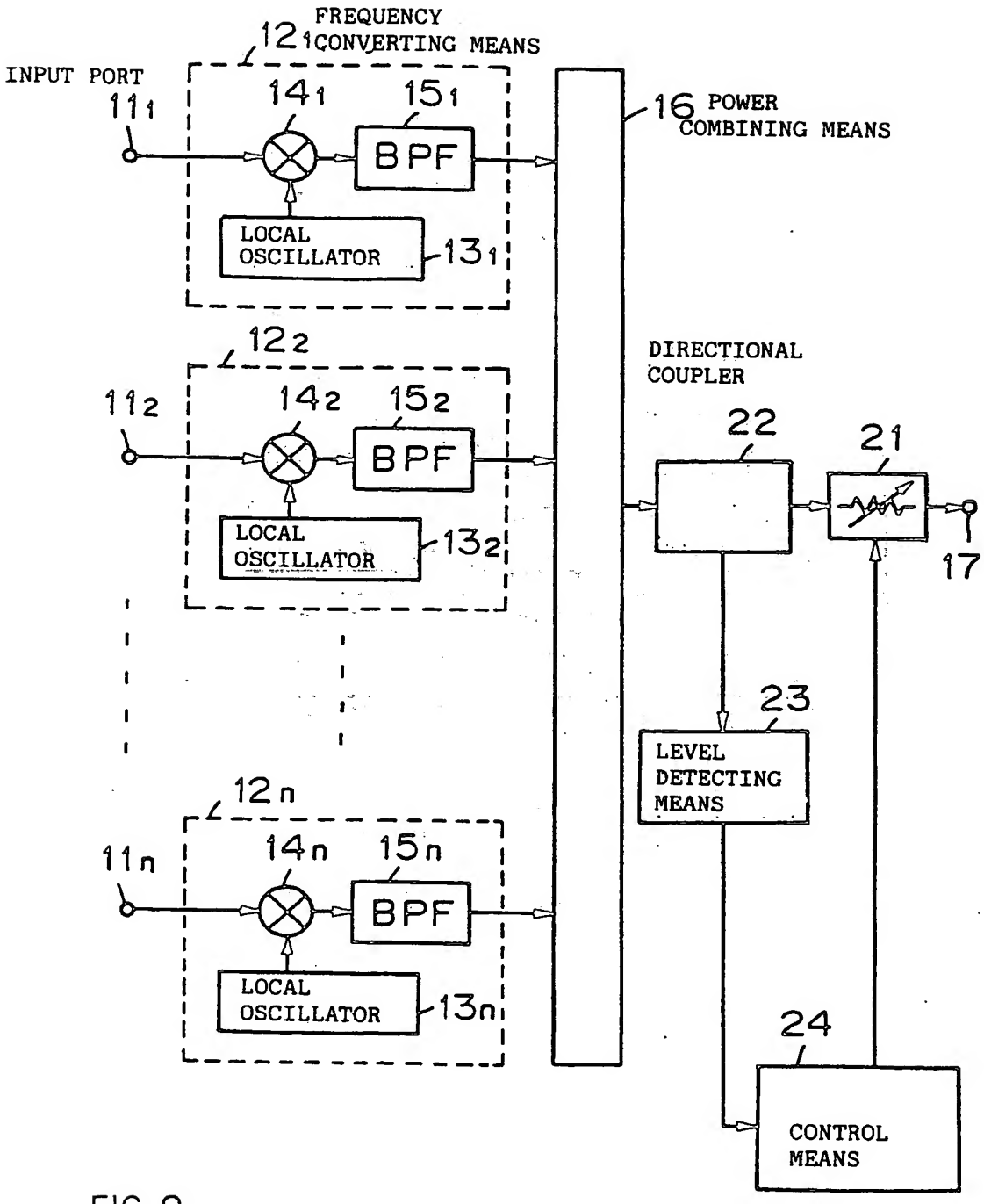

FREQUENCY
CONVERTING MEANS
INPUT PORT
11_1
12_1
14_1
15_1
BPF
LOCAL OSCILLATOR
13_1
12_2
11_2
14_2
15_2
BPF
LOCAL OSCILLATOR
13_2
12_n
11_n
14_n
15_n
BPF
LOCAL OSCILLATOR
13_n
16 POWER COMBINING MEANS
DIRECTIONAL COUPLER
22
21
17
23
LEVEL DETECTING MEANS
24
CONTROL MEANS

FIG. 9

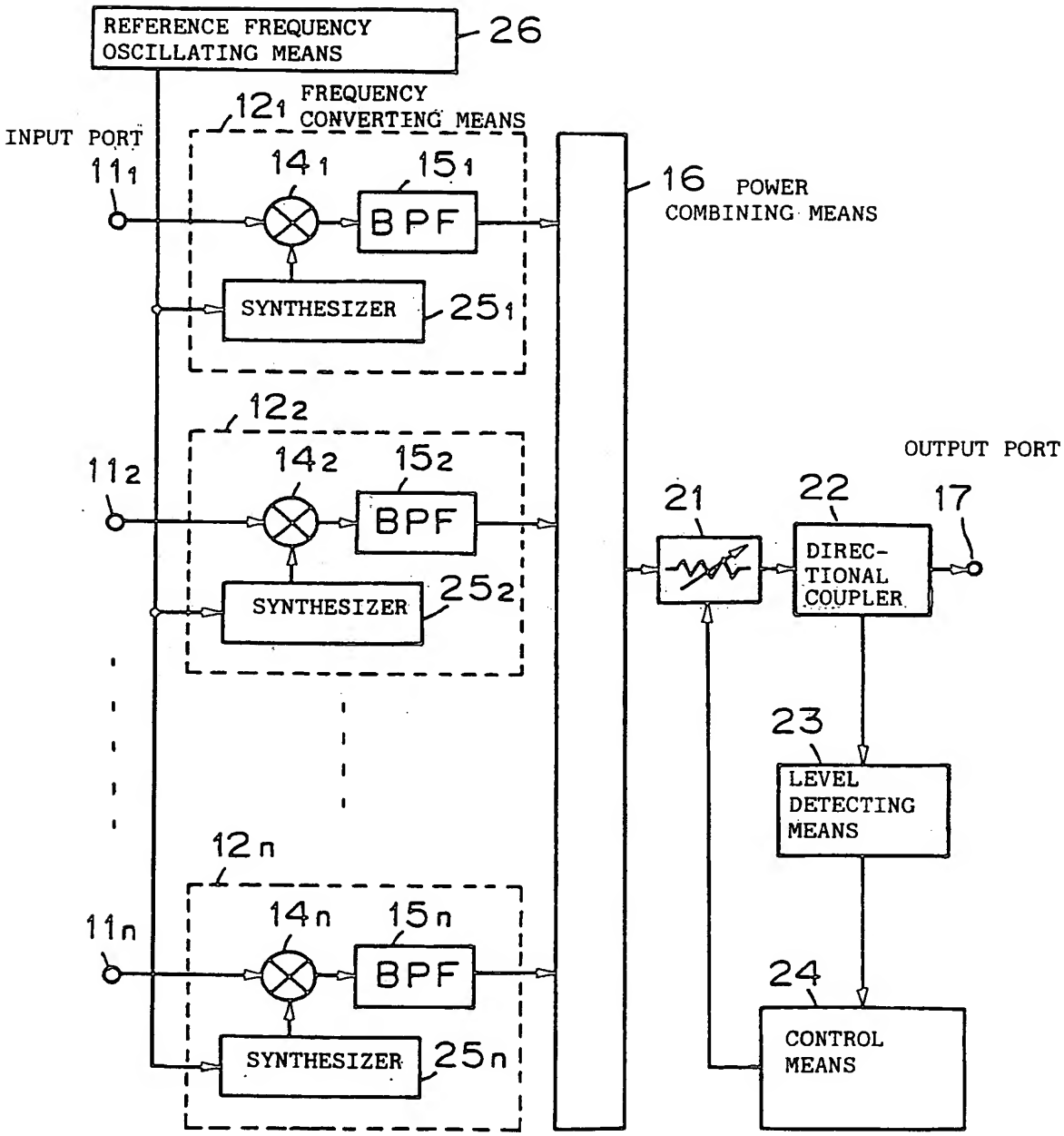
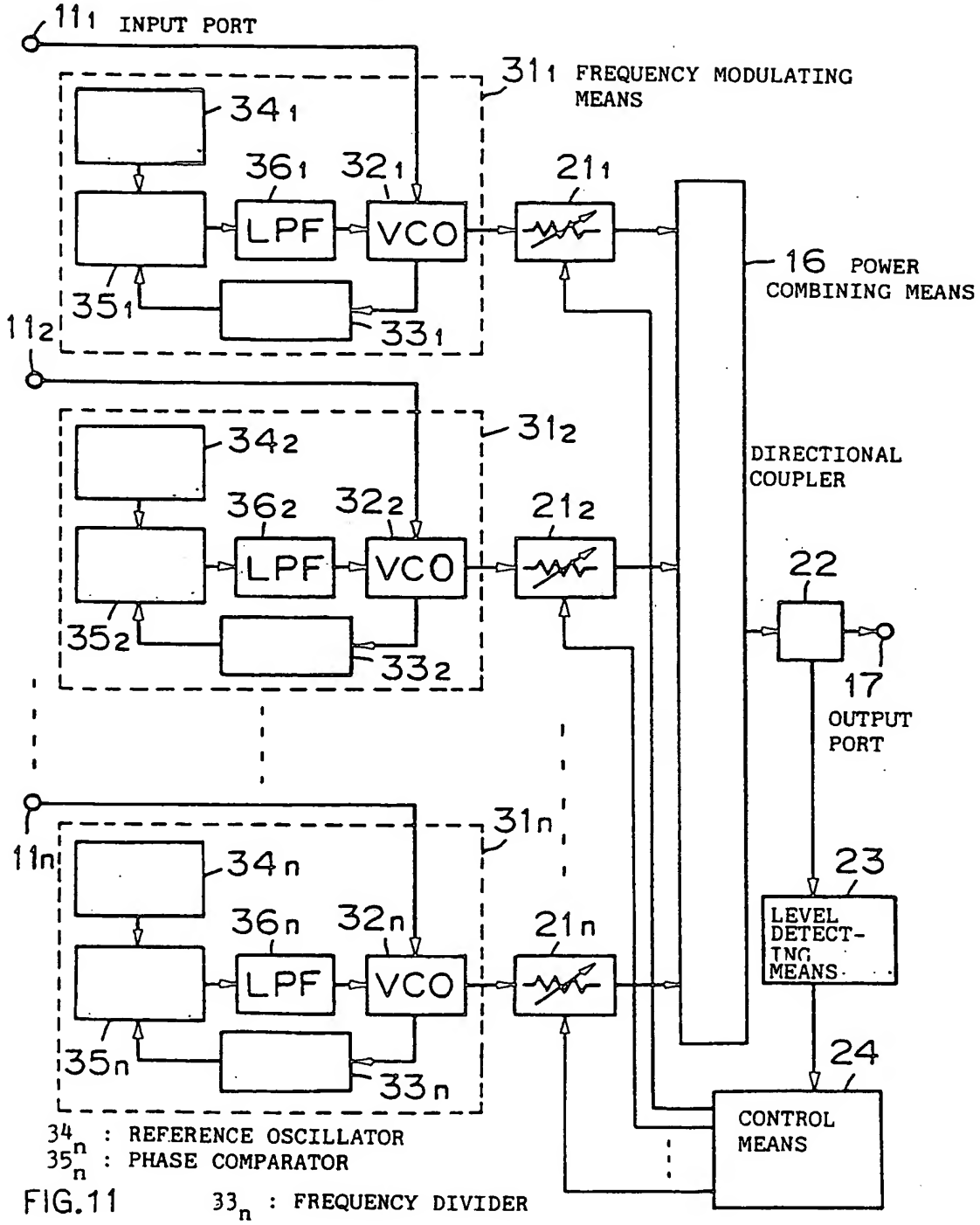

REFERENCE FREQUENCY OSCILLATING MEANS
26
FREQUENCY CONVERTING MEANS
INPUT PORT
BPF
SYNTHESIZER
16 POWER COMBINING MEANS
OUTPUT PORT
21
22
17
DIREC-TIONAL COUPLER
23
LEVEL DETECTING MEANS
24
CONTROL MEANS

FIG.10

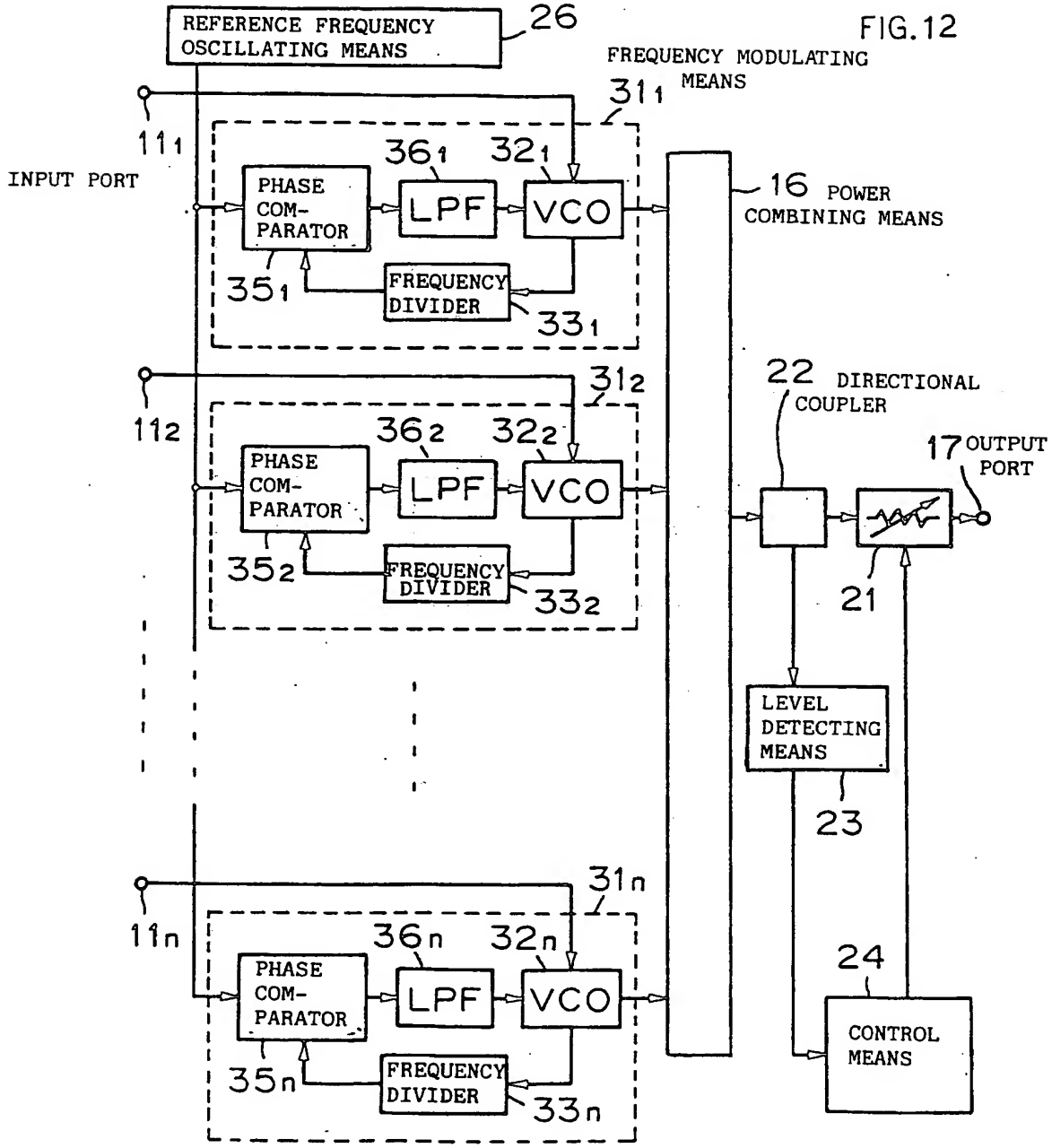
34_1, 34_2 : REFERENCE OSCILLATOR
35_1, 35_2 : PHASE COMPARATOR
33_1, 33_2 : FREQUENCY DIVIDER



34_n : REFERENCE OSCILLATOR
35_n : PHASE COMPARATOR

FIG.11 33_n : FREQUENCY DIVIDER

FIG.12



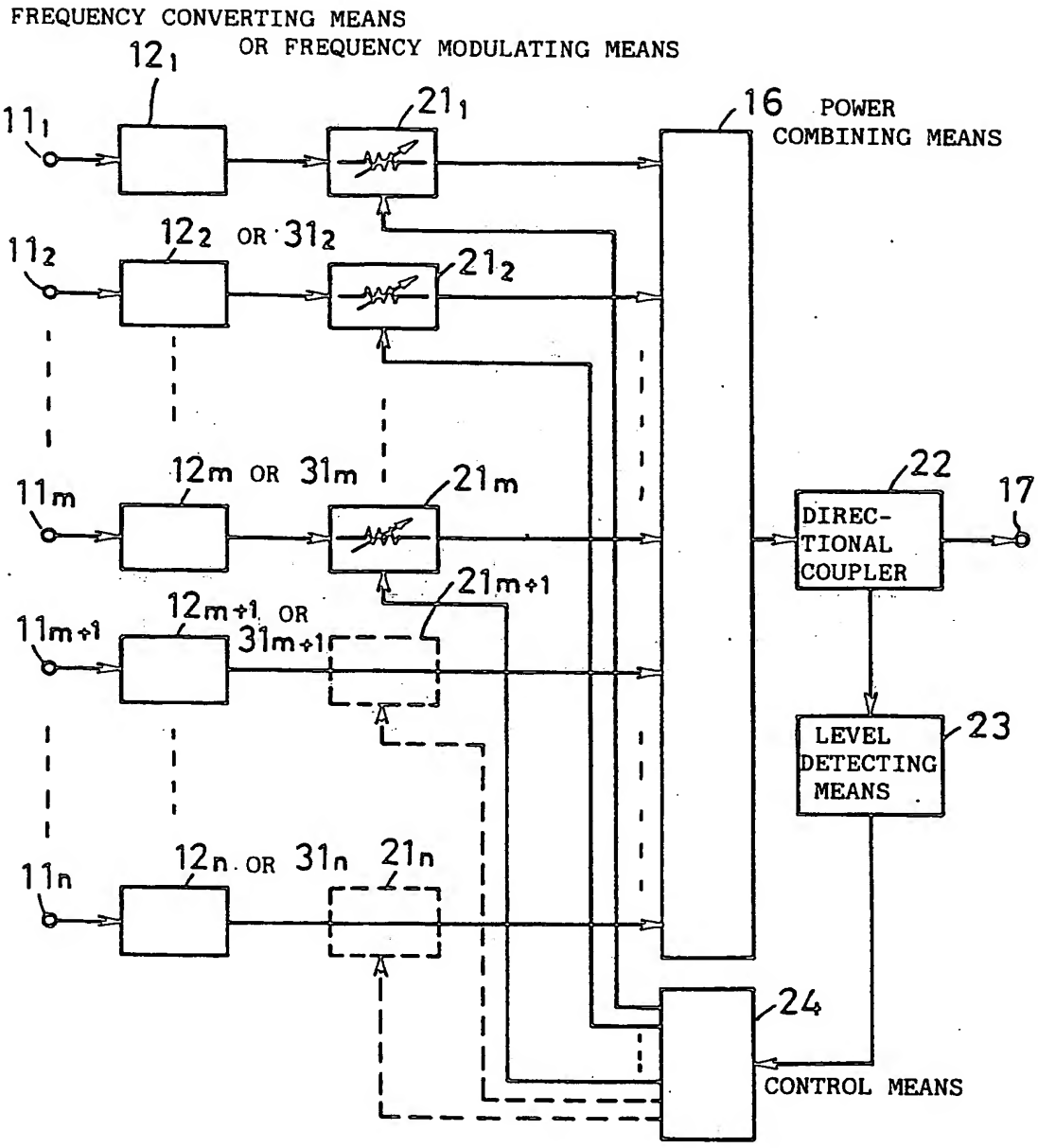


FIG. 13

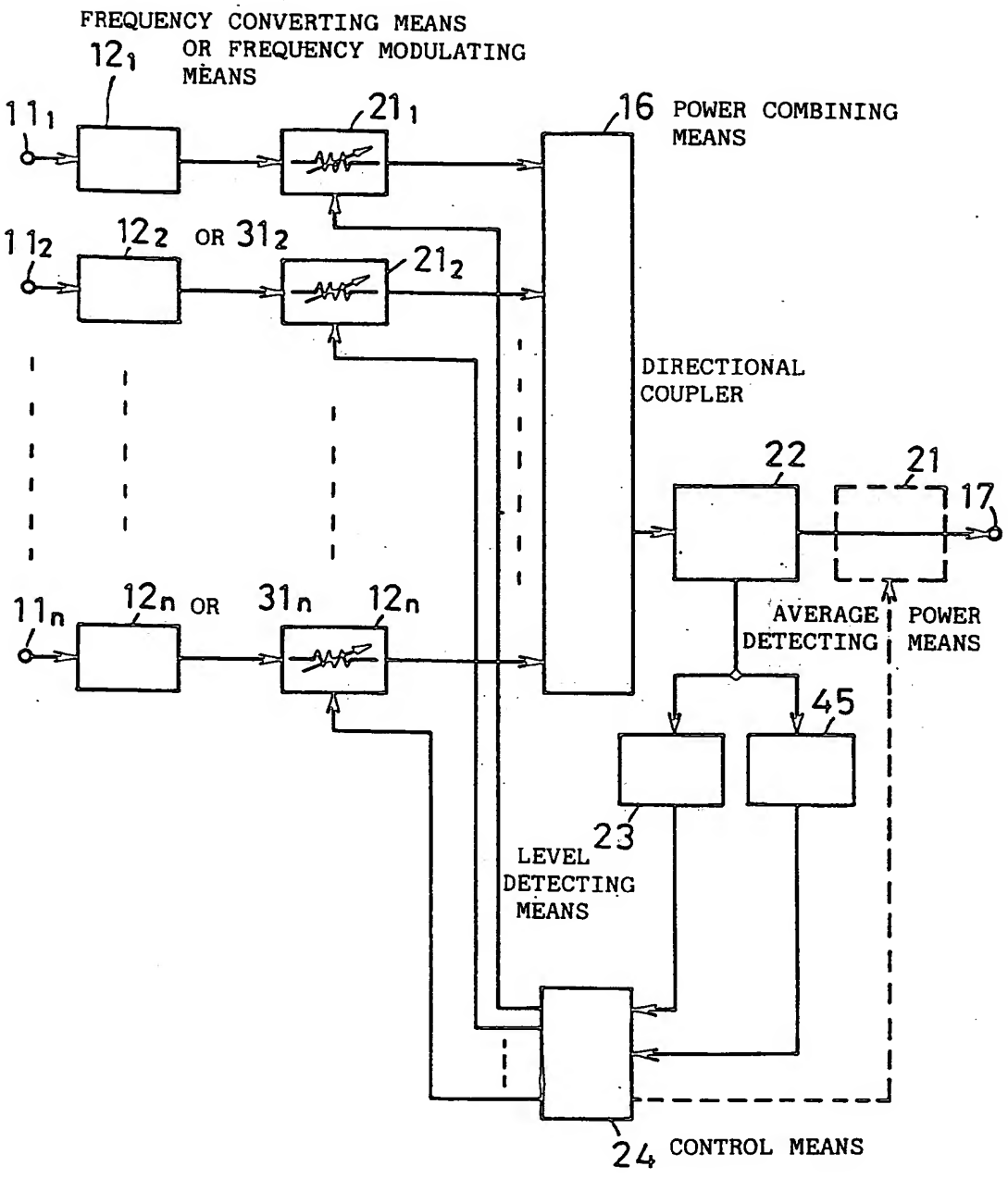

FREQUENCY CONVERTING MEANS
OR FREQUENCY MODULATING
MEANS
12_1
11_1
21_1
16
POWER COMBINING
MEANS
11_2
12_2
OR 31_2
21_2
DIRECTIONAL
COUPLER
22
21
17
11_n
12_n OR
31_n
12_n
AVERAGE
DETECTING
POWER
MEANS
45
23
LEVEL
DETECTING
MEANS
24
CONTROL MEANS

FIG.14

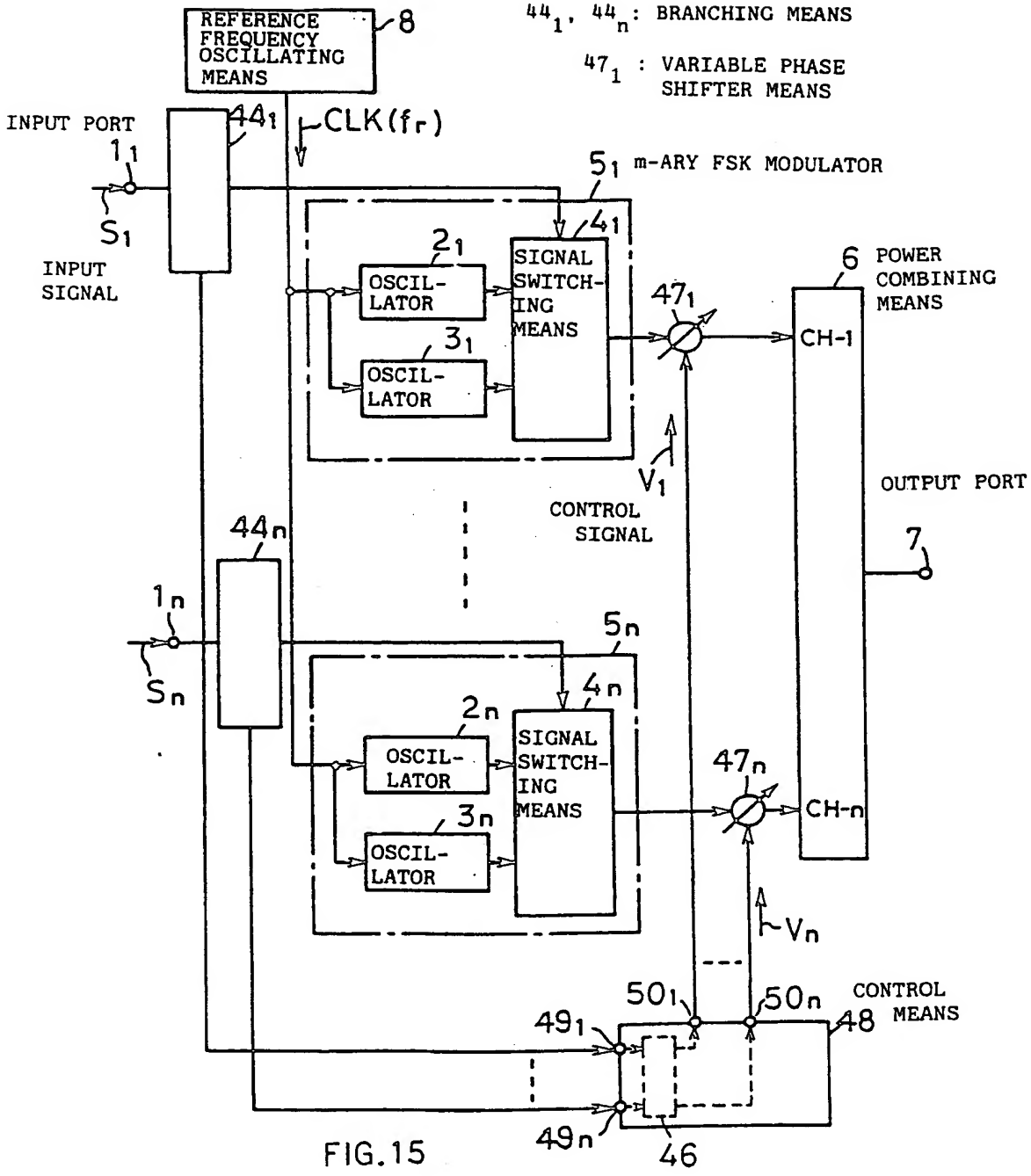

REFERENCE FREQUENCY OSCILLATING MEANS
8
44_1, 44_n: BRANCHING MEANS
47_1 : VARIABLE PHASE SHIFTER MEANS
INPUT PORT
1_1
44_1
CLK(f_r)
5_1 m-ARY FSK MODULATOR
S_1
INPUT SIGNAL
2_1
OSCIL-LATOR
3_1
OSCIL-LATOR
4_1
SIGNAL SWITCH-ING MEANS
47_1
6
POWER COMBINING MEANS
CH-1
V_1
CONTROL SIGNAL
OUTPUT PORT
7
44_n
1_n
5_n
S_n
2_n
OSCIL-LATOR
3_n
OSCIL-LATOR
4_n
SIGNAL SWITCH-ING MEANS
47_n
CH-n
V_n
50_1
50_n
CONTROL MEANS
48
49_1
49_n
46

FIG.15

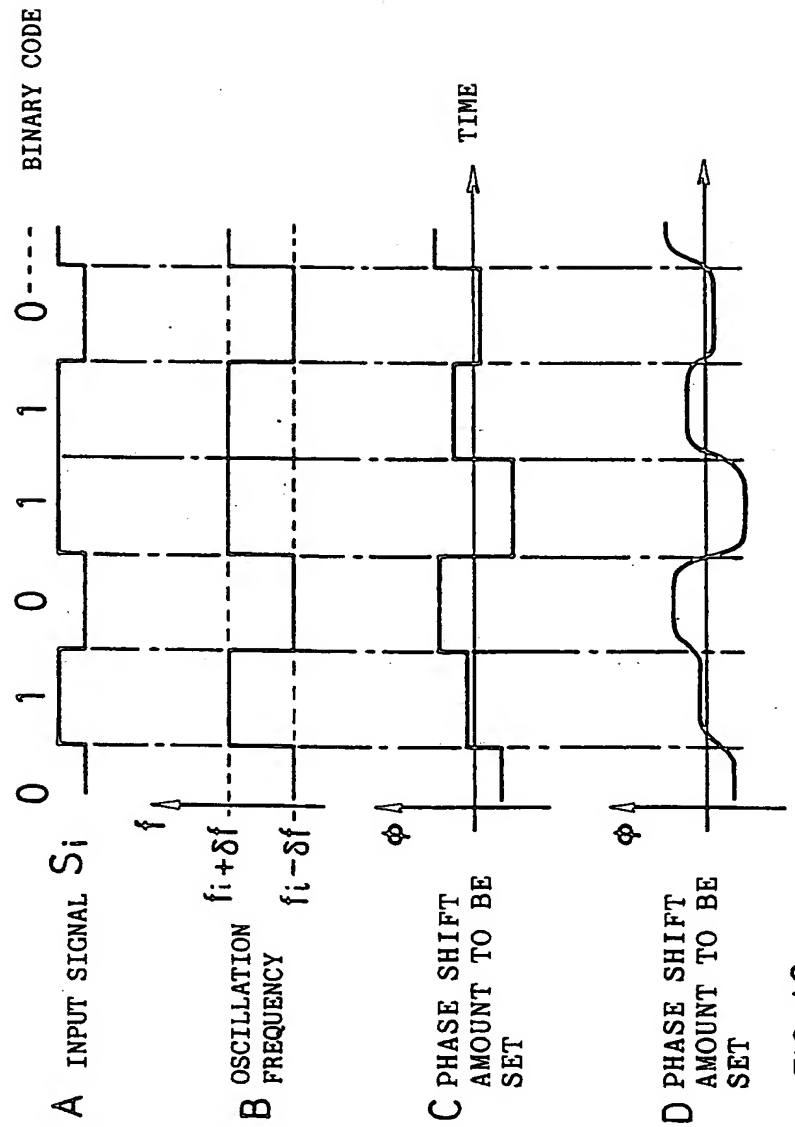


FIG. 16

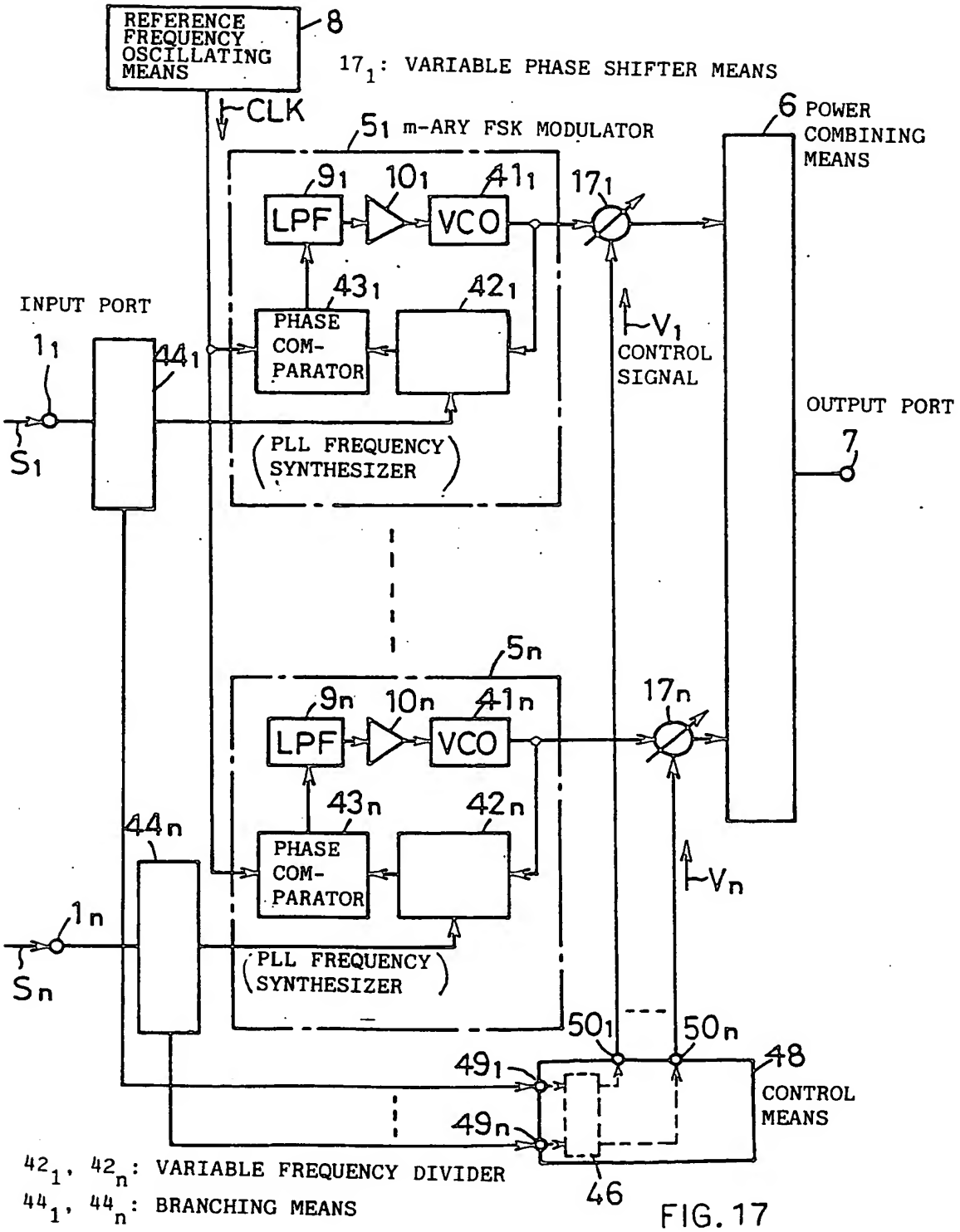

REFERENCE FREQUENCY OSCILLATING MEANS
8
17_1: VARIABLE PHASE SHIFTER MEANS
CLK
5_1 m-ARY FSK MODULATOR
6 POWER COMBINING MEANS
9_1
10_1
41_1
17_1
LPF
VCO
43_1
42_1
INPUT PORT
1_1
44_1
PHASE COM-PARATOR
V_1 CONTROL SIGNAL
OUTPUT PORT
7
S_1
PLL FREQUENCY SYNTHESIZER
5_n
9_n
10_n
41_n
17_n
LPF
VCO
43_n
42_n
44_n
PHASE COM-PARATOR
V_n
1_n
S_n
PLL FREQUENCY SYNTHESIZER
50_1
50_n
49_1
48
CONTROL MEANS
49_n
46
42_1, 42_n: VARIABLE FREQUENCY DIVIDER
44_1, 44_n: BRANCHING MEANS

FIG. 17

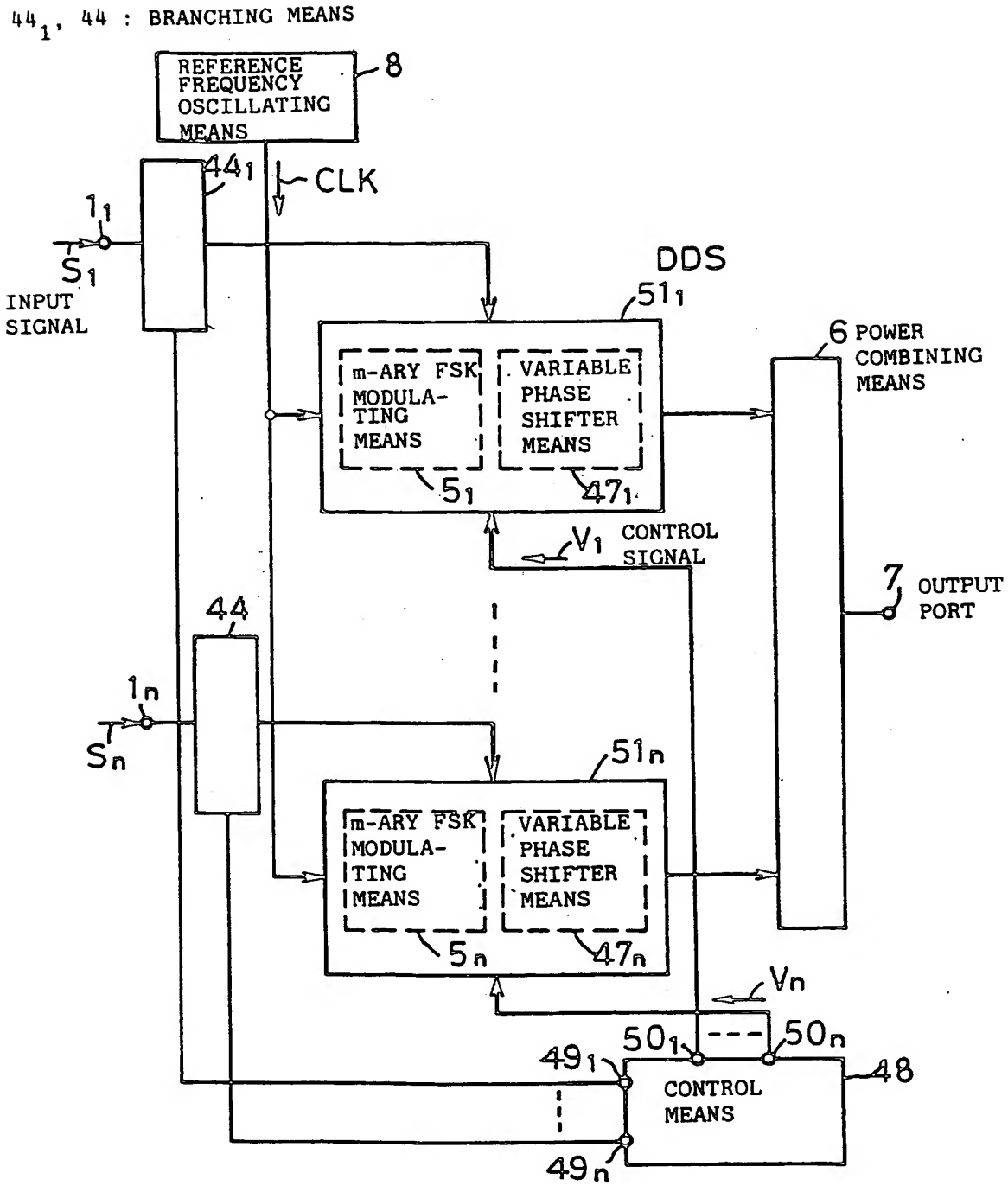

44_1, 44 : BRANCHING MEANS
REFERENCE FREQUENCY OSCILLATING MEANS
8
44_1
CLK
1_1
S_1
INPUT SIGNAL
DDS
51_1
m-ARY FSK MODULA-TING MEANS
VARIABLE PHASE SHIFTER MEANS
5_1
47_1
6 POWER COMBINING MEANS
V_1 CONTROL SIGNAL
7 OUTPUT PORT
44
1_n
S_n
51_n
m-ARY FSK MODULA-TING MEANS
VARIABLE PHASE SHIFTER MEANS
5_n
47_n
V_n
50_1
50_n
49_1
49_n
CONTROL MEANS
48

FIG. 18

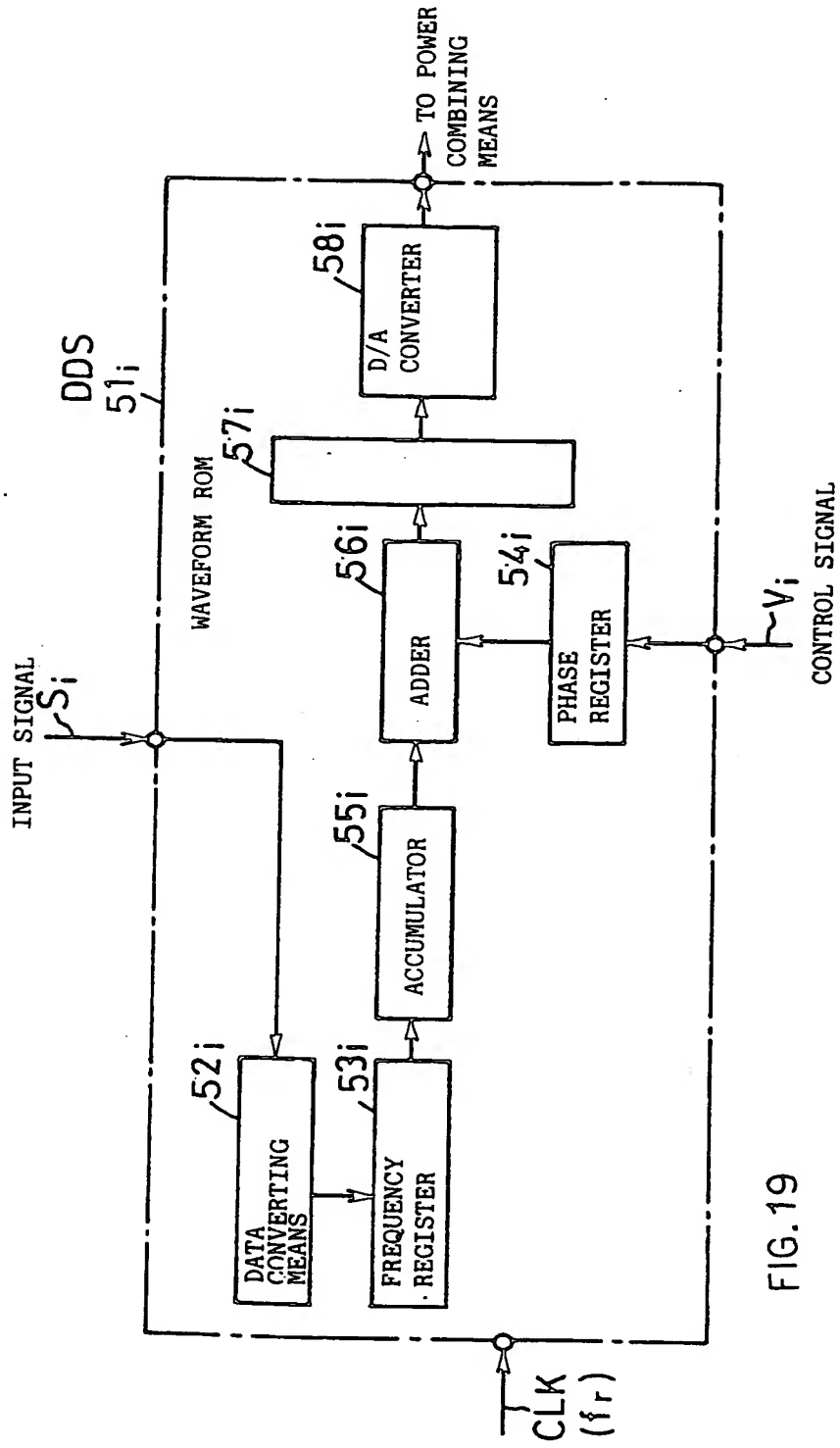


FIG. 19

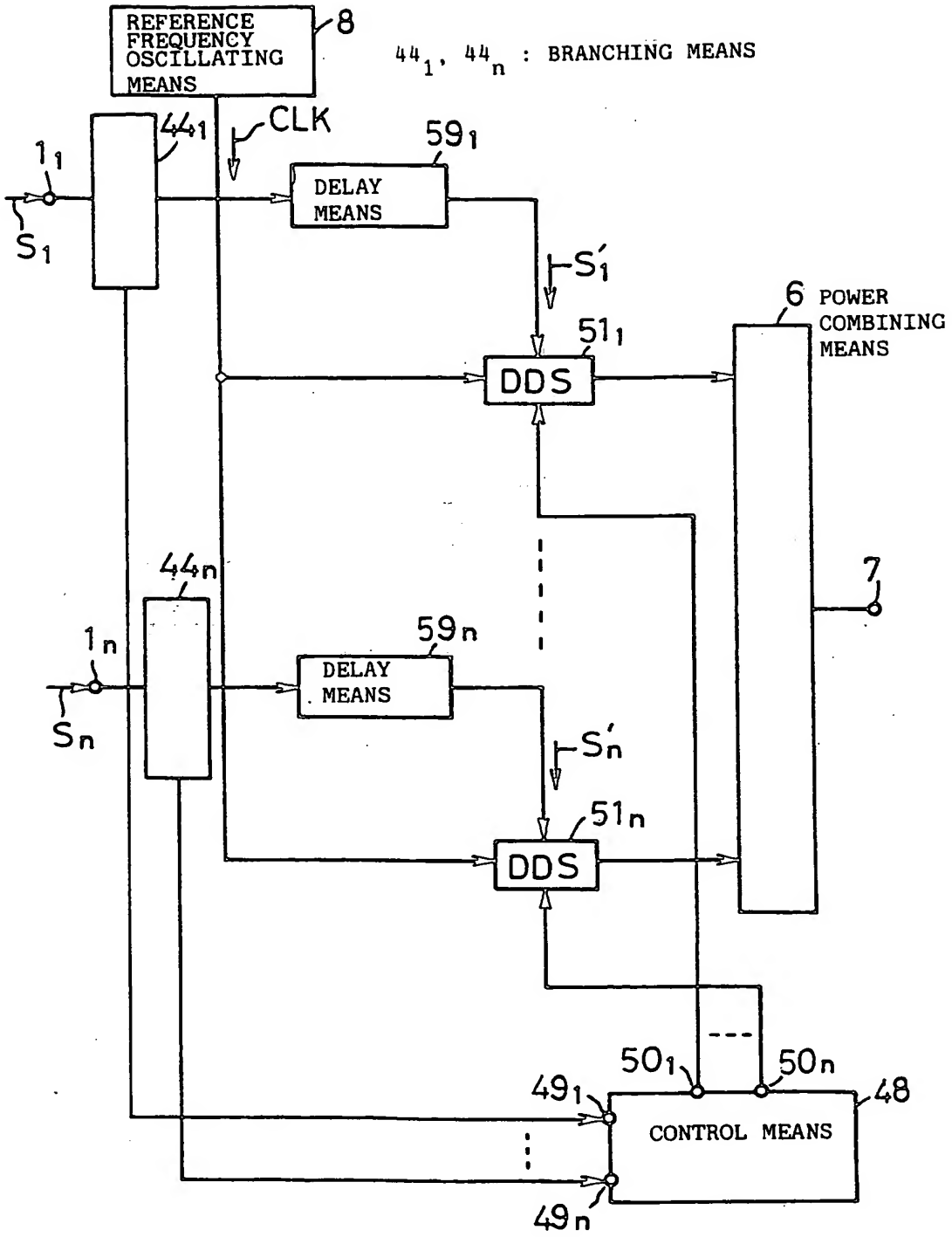

REFERENCE FREQUENCY OSCILLATING MEANS
8
44_1, 44_n : BRANCHING MEANS
CLK
44_1
59_1
1_1
S_1
DELAY MEANS
S'_1
51_1
DDS
6 POWER COMBINING MEANS
7
44_n
1_n
59_n
DELAY MEANS
S_n
S'_n
51_n
DDS
50_1
50_n
49_1
48
CONTROL MEANS
49_n

FIG. 20

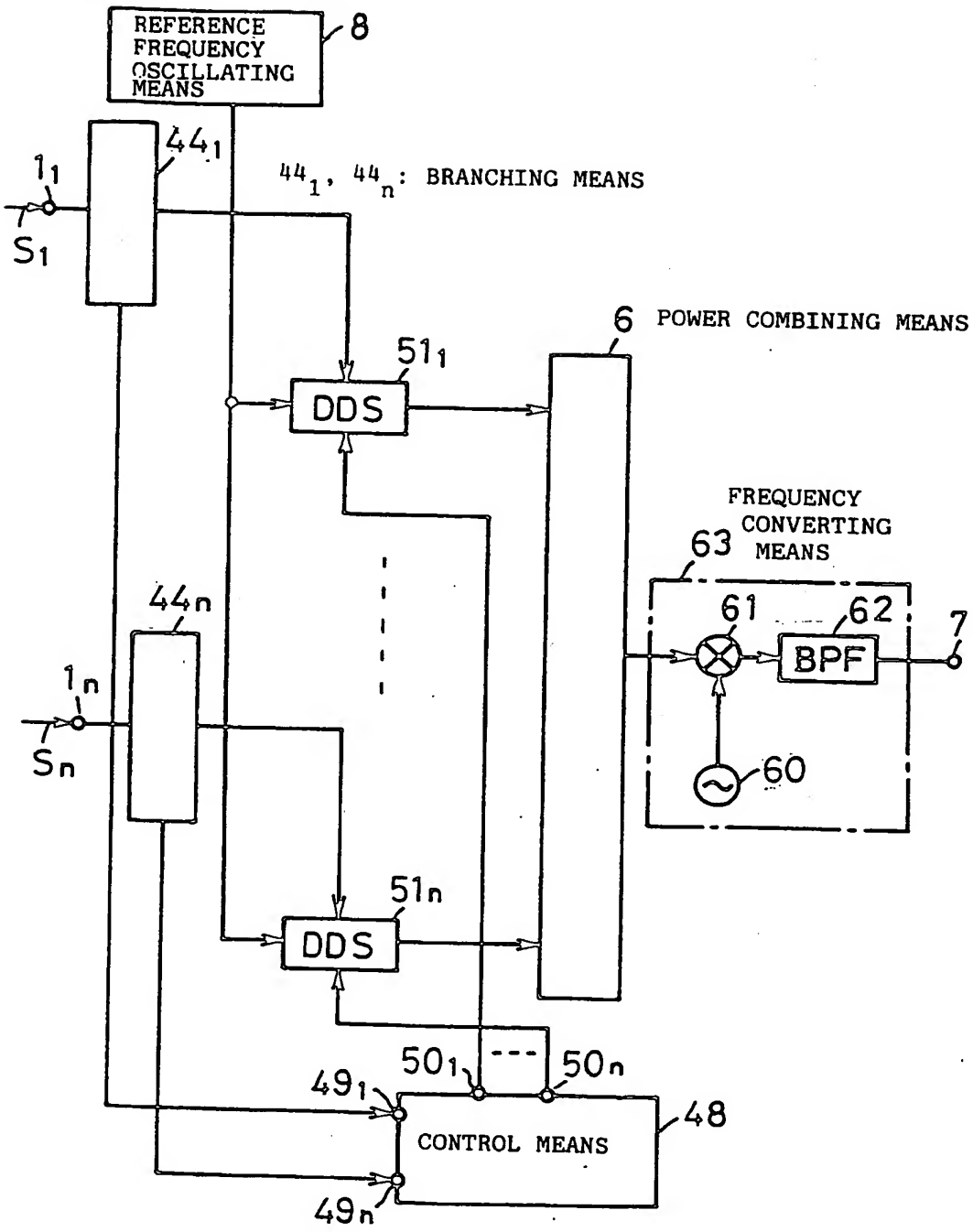


FIG. 21

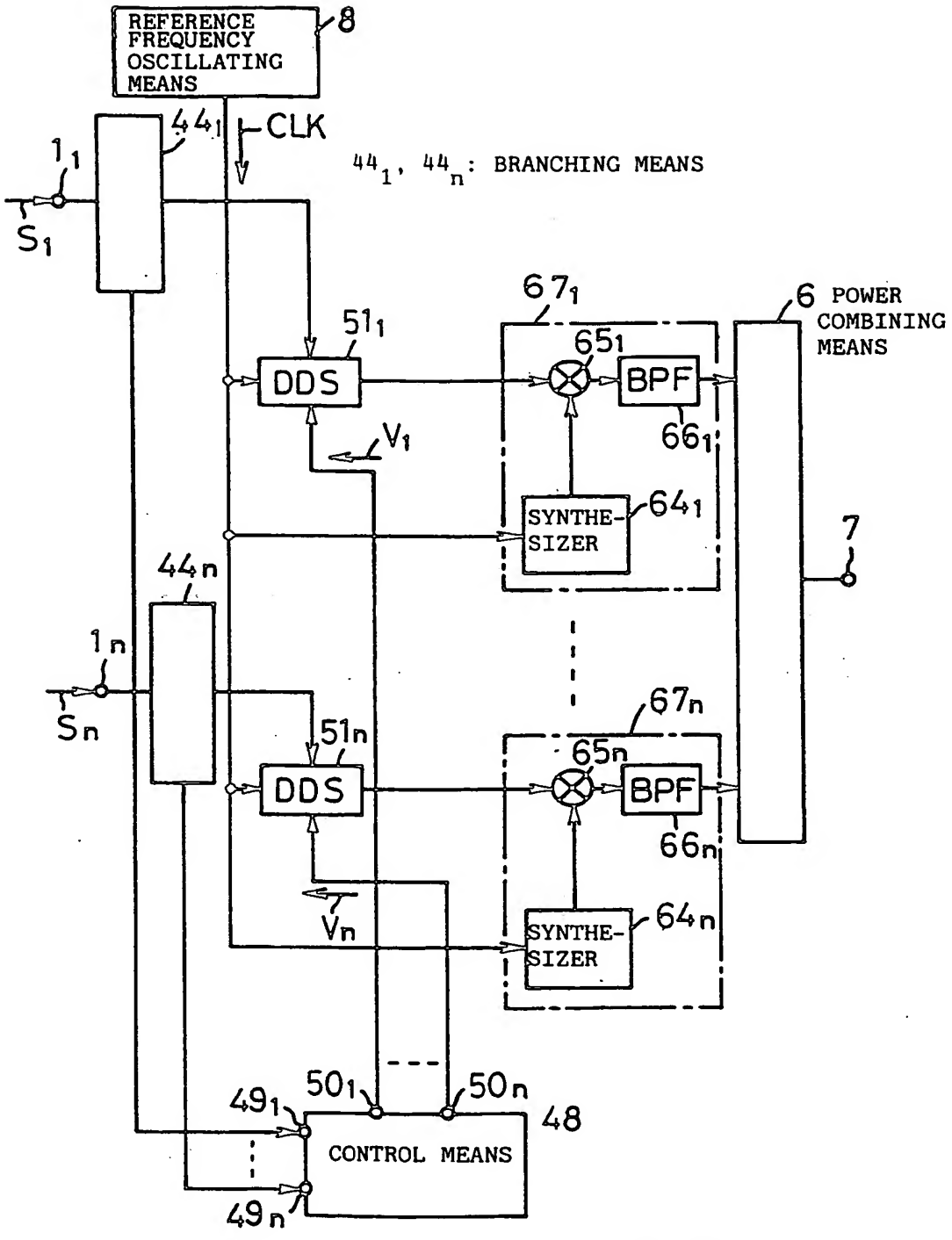

REFERENCE FREQUENCY OSCILLATING MEANS
8
CLK
44_1, 44_n: BRANCHING MEANS
1_1
S_1
44_1
51_1
DDS
V_1
67_1
65_1
BPF
66_1
SYNTHE-SIZER
64_1
6 POWER COMBINING MEANS
7
44_n
1_n
S_n
51_n
DDS
V_n
67_n
65_n
BPF
66_n
SYNTHE-SIZER
64_n
50_1
50_n
49_1
49_n
CONTROL MEANS
48

FIG. 22

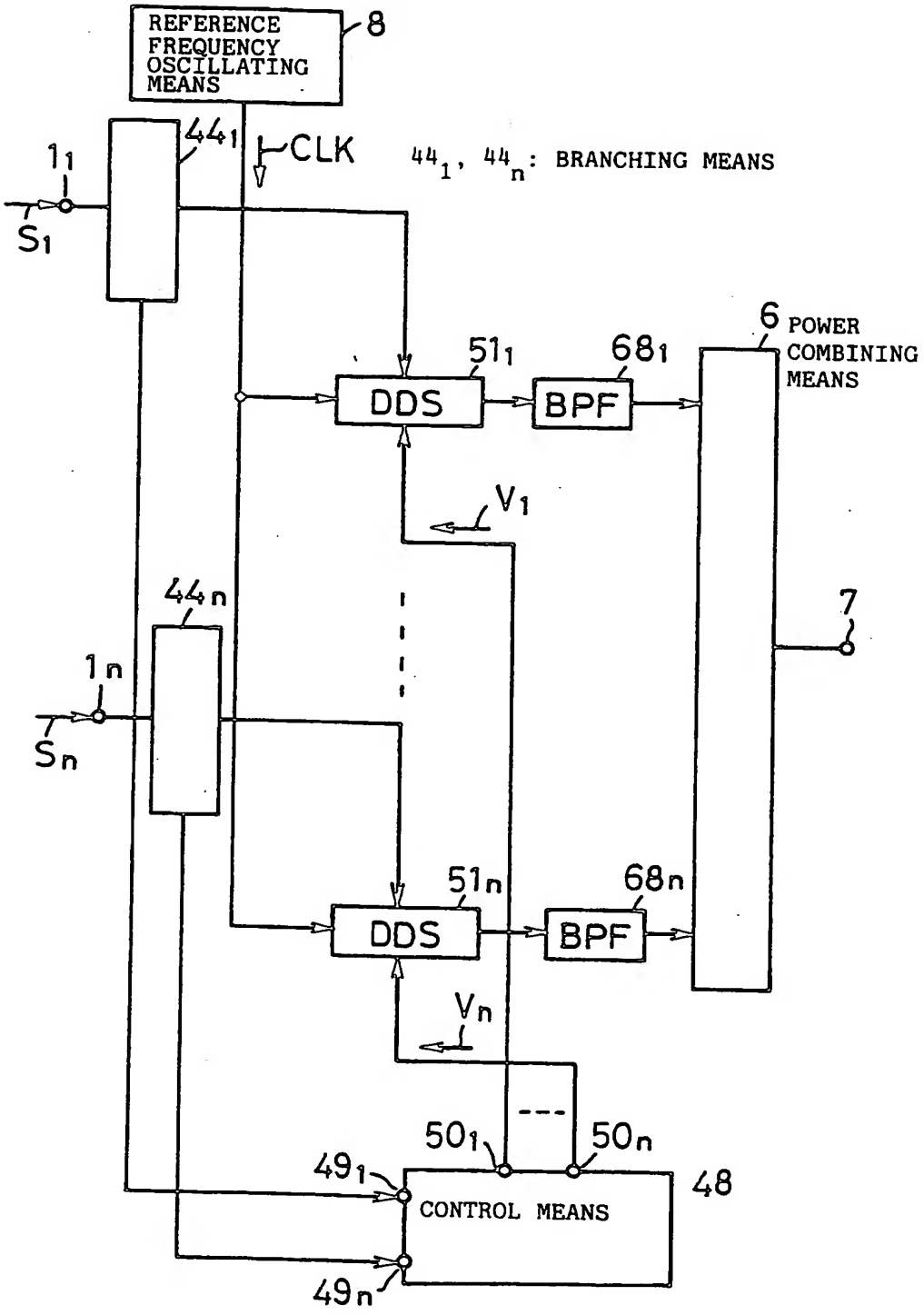

REFERENCE FREQUENCY OSCILLATING MEANS
8
CLK
44_1, 44_n: BRANCHING MEANS
1_1
S_1
44_1
51_1
68_1
DDS
BPF
6
POWER COMBINING MEANS
V_1
44_n
1_n
S_n
7
51_n
68_n
DDS
BPF
V_n
50_1
50_n
49_1
48
CONTROL MEANS
49_n

FIG. 23

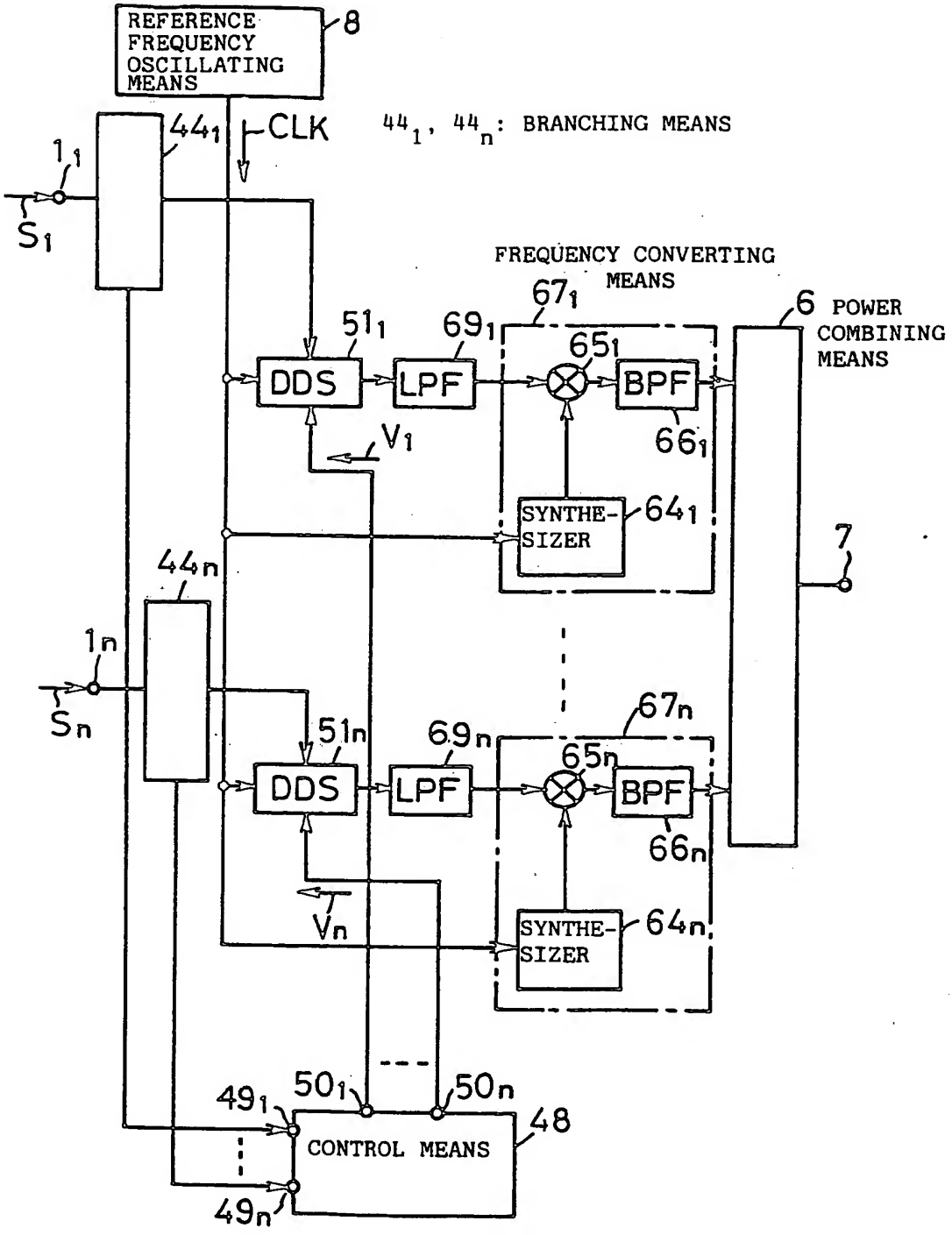


FIG. 24

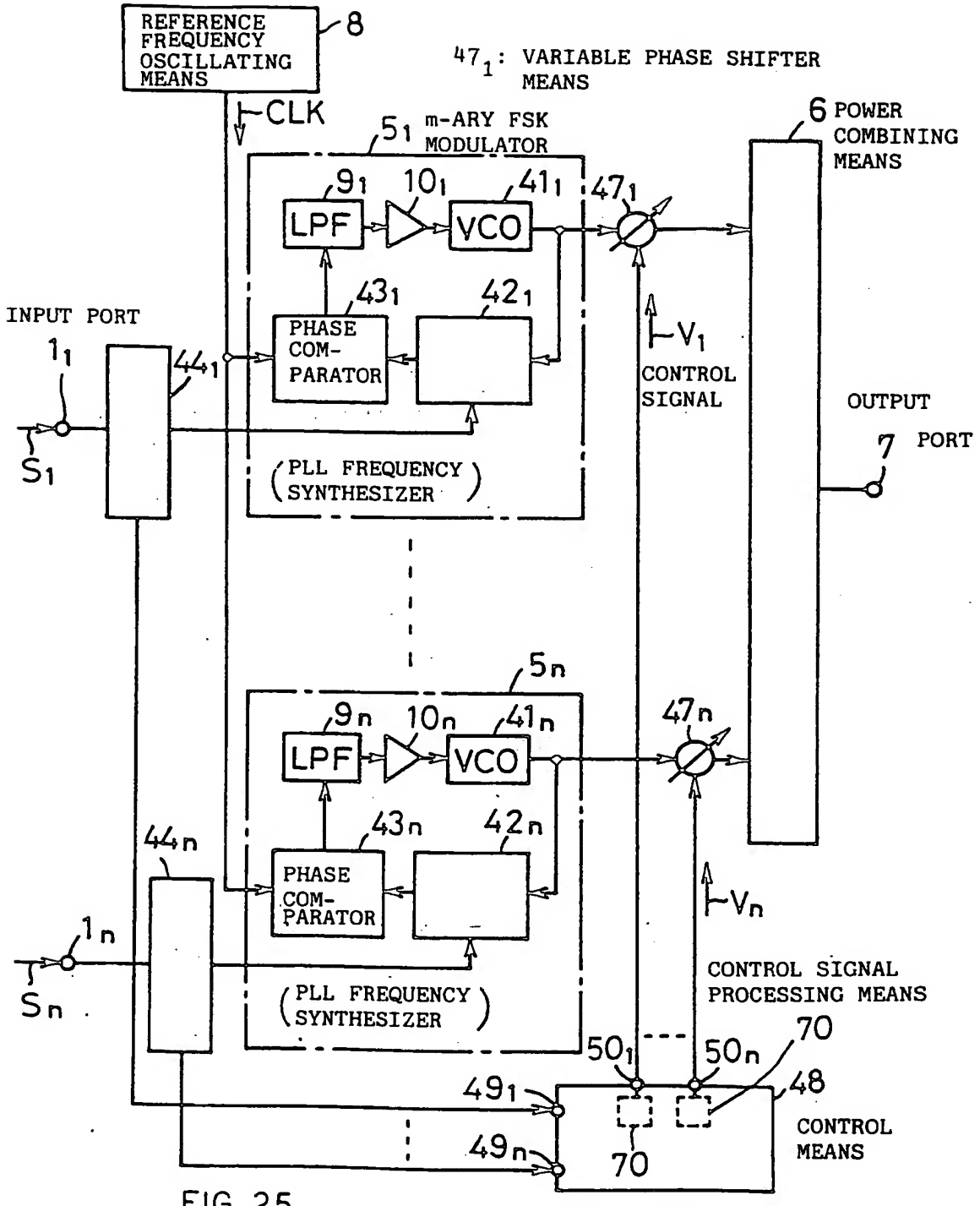


FIG.25

42_1, 42_n: VARIABLE FREQUENCY DIVIDER

44_1, 44_n: BRANCHING MEANS

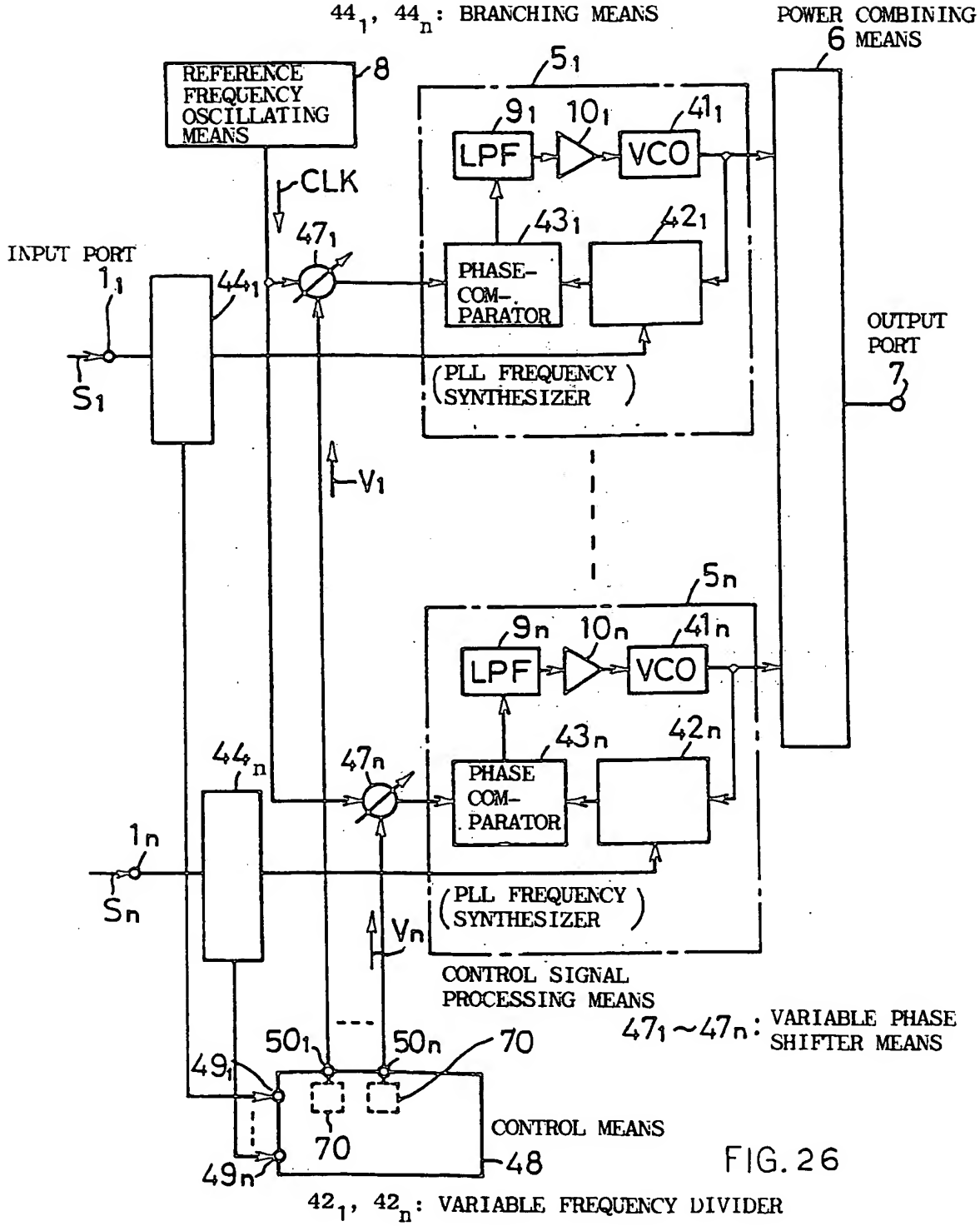


FIG. 26

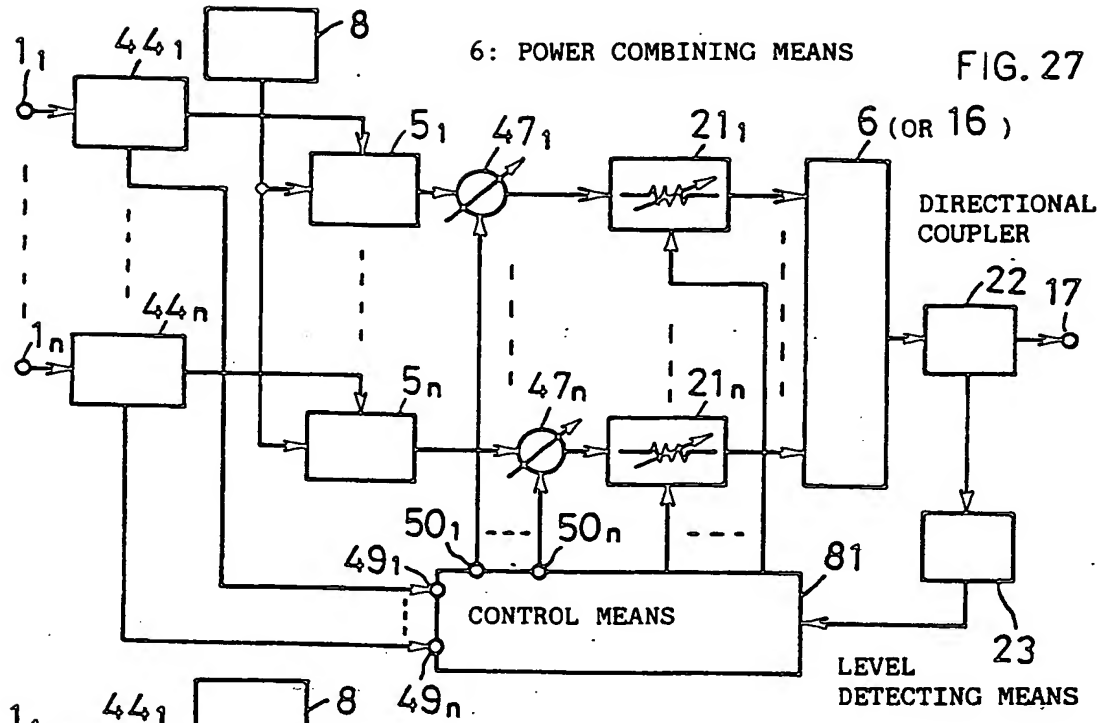


FIG. 27

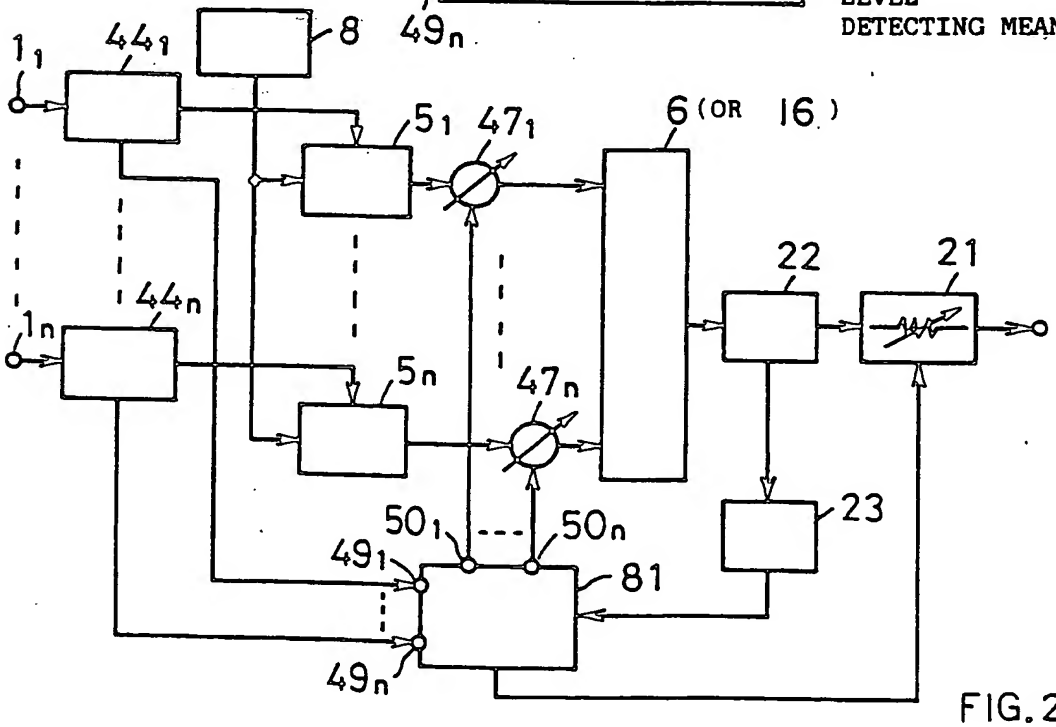


FIG. 28

FIG. 29

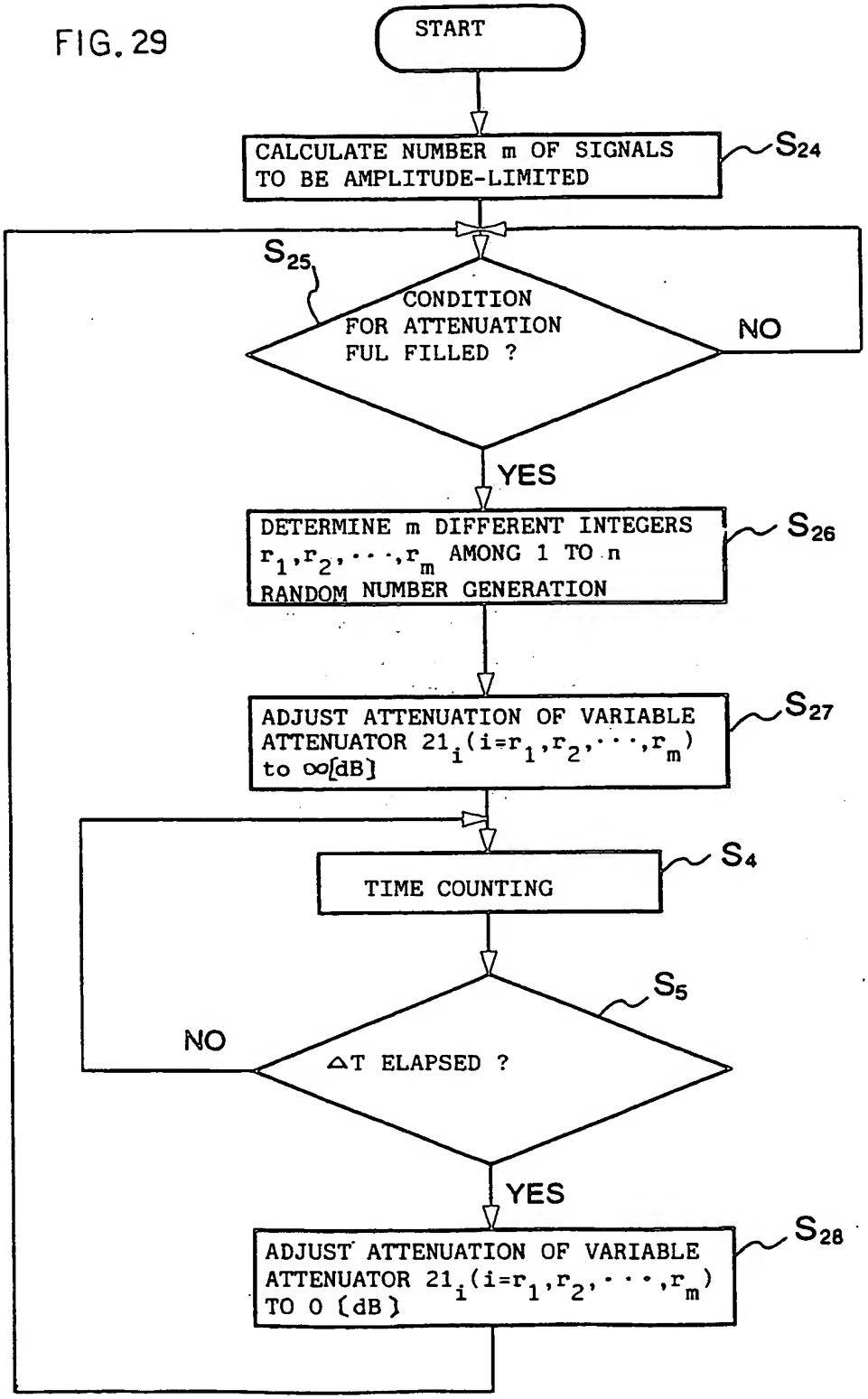
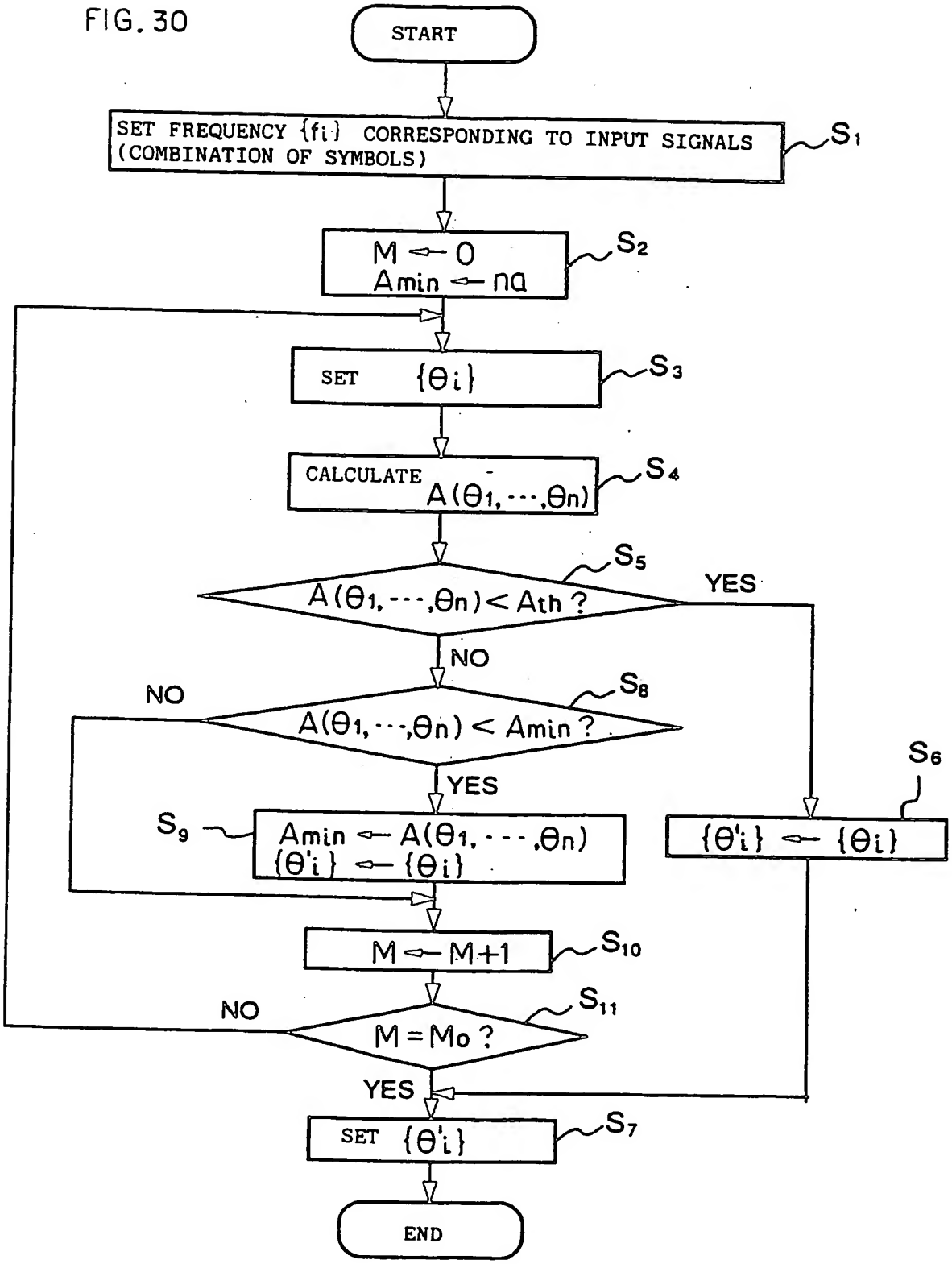


FIG. 30



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP95/02467

A. CLASSIFICATION OF SUBJECT MATTER
Int. Cl^6 H04J1/00, H04B1/04, H04L27/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int. Cl^6 H04J1/00, H04B1/04, H04L27/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926 - 1995
Kokai Jitsuyo Shinan Koho 1971 - 1995

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 6-132835, A2 (NEC Corp.), May 13, 1994 (13. 05. 94), Fig. 1 (Family: none)	1-9, 13-17, 19-20, 22-23, 39
A	JP, 4-355527, A (NEC Corp.), December 9, 1992 (09. 12. 92), Fig. 1 1A, 1B, 1C, 13, 5 (Family: none)	1-9, 13-17, 19-20, 22-23, 31, 39
A	JP, 59-154826, A2 (NEC Corp.), September 3, 1984 (03. 09. 84), Line 15, upper left column to line 7, lower left column, page 2 (Family: none)	10-16, 18, 21-23, 40
A	JP, 1-238331, A2 (Fujitsu Ltd.), September 22, 1989 (22. 09. 89), Figs. 2, 5 (Family: none)	10-16, 18, 21-40
A	JP, 64-69131, A2 (Fujitsu Ltd.), March 15, 1989 (15. 03. 89), Fig. 2 (Family: none)	24 - 40

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
February 9, 1996 (09. 02. 96)	March 5, 1996 (05. 03. 96)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP95/02467

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 6-204773, A2 (American Telephone & Telegraph Co.), July 22, 1994 (22. 07. 94), Fig. 1 153 & US, 5300894, A & EP, 594352, A2	1-16, 19-40
A	JP, 6-204959, A2 (American Telephone & Telegraph Co.), July 22, 1994 (22. 07. 94), Fig. 1 152, 153 & US, 5302914, A & EP, 594358, A3 & AU, 655375, B2	17-18, 24-40

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